PATENTED
PAT No. : TW 099352

Features

- Operating voltage: 2.4V~5.5V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- Package types
  - HT1621S: 44-pin LQFP and 48-pin SSOP/LQFP
  - HT1621SG: Gold bumped chip

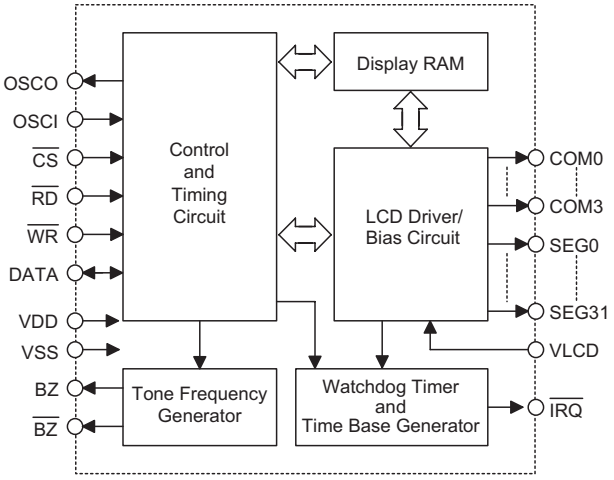
General Description

The HT1621S is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the HT1621S makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the HT1621S. The HT1621S contains a power down command to reduce power consumption.

Selection Table

HT162x	HT1620	HT1621	HT1621S	HT1622	HT16220	HT1623	HT1625	HT1626
COM	4	4	**4**	8	8	8	8	16
SEG	32	32	**32**	32	32	48	64	48
Built-in Osc.	—	√	√	√	—	√	√	√
Crystal Osc.	√	√	√	—	√	√	√	√

Block Diagram



Note: $\overline{CS}$: Chip selection

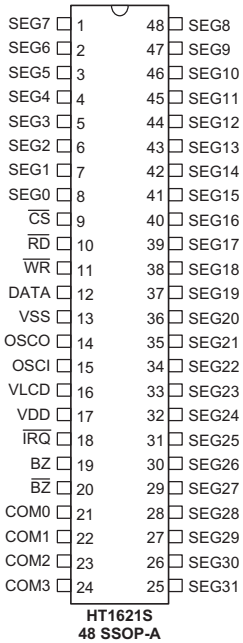
BZ, $\overline{BZ}$: Tone outputs

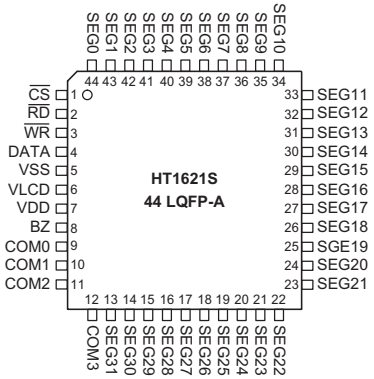
$\overline{WR}$, $\overline{RD}$, DATA: Serial interface

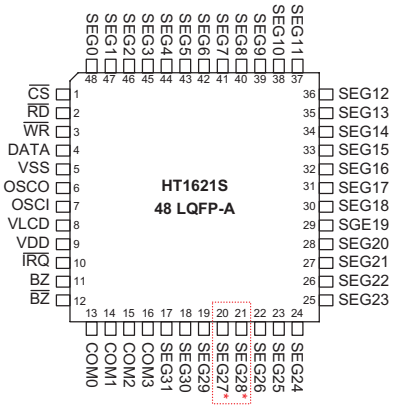
COM0~COM3, SEG0~SEG31: LCD outputs

$\overline{IRQ}$: Time base or WDT overflow output

Pin Assignment

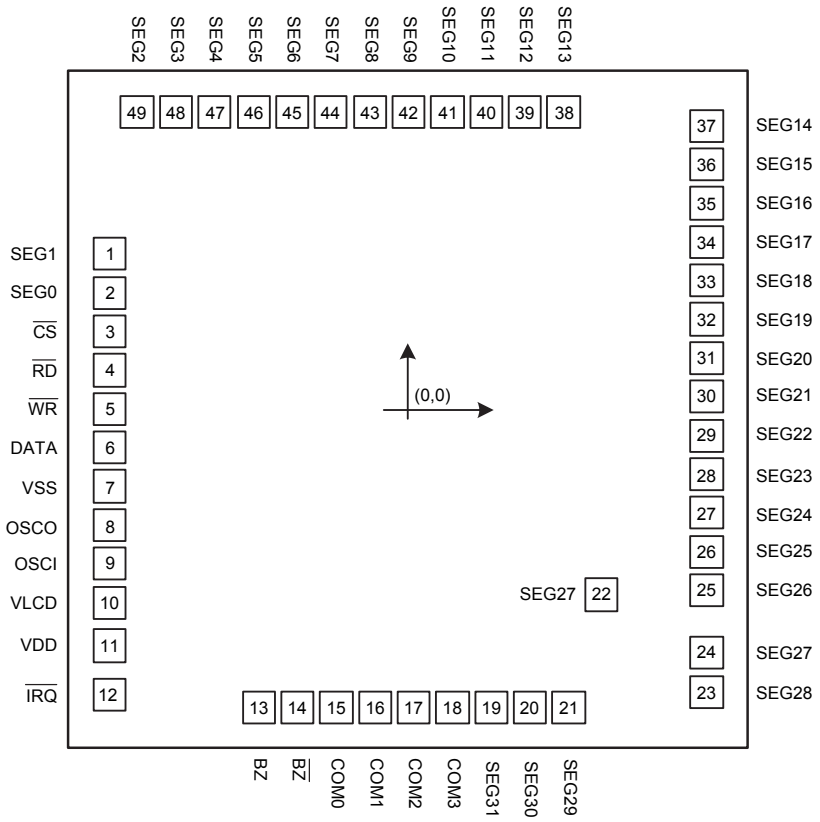






Note: * Please note that in the 48-pin LQFP package, the SEG27 and SEG28 pins are not in sequential order.

Pad Assignment



Chip size: 1328 × 1326 μm

* The IC substrate should be connected to VSS in the PCB layout artwork.

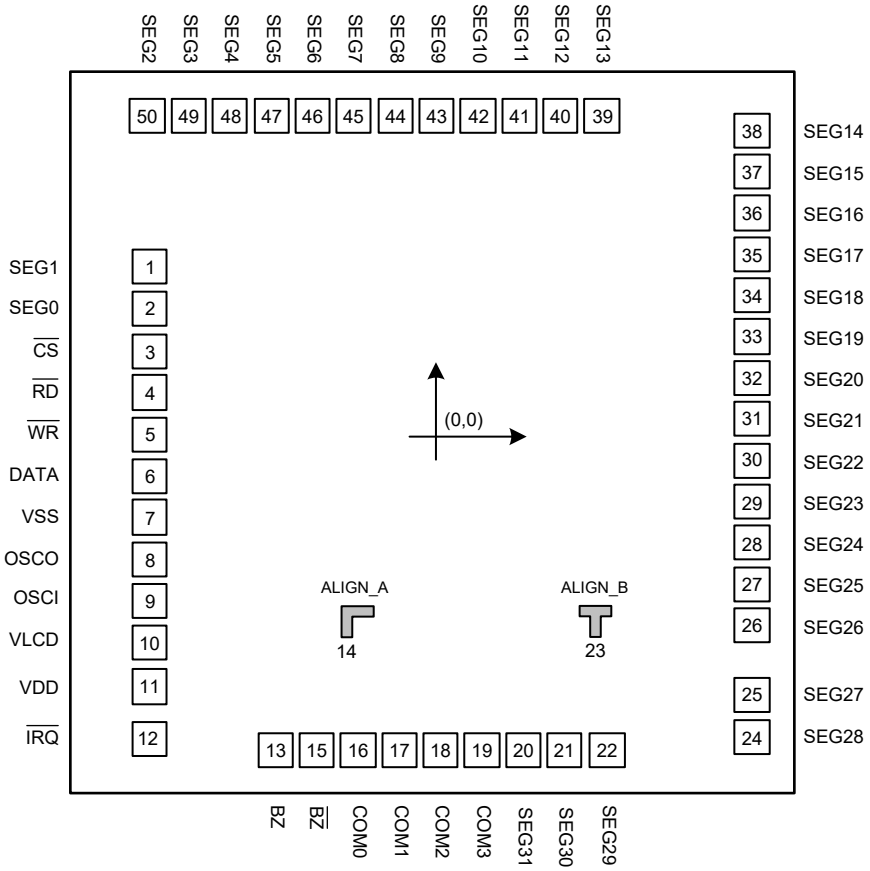
Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	-577.500	300.780	26	577.500	-275.445
2	-577.500	225.780	27	577.500	-200.445
3	-577.500	150.780	28	577.500	-125.445
4	-577.500	75.780	29	577.500	-50.445
5	-577.500	0.780	30	577.500	24.555
6	-577.500	-74.220	31	577.500	99.555
7	-577.500	-149.220	32	577.500	174.555
8	-577.500	-224.220	33	577.500	249.555
9	-577.500	-299.220	34	577.500	324.555
10	-577.500	-374.220	35	577.500	399.555
11	-577.500	-457.465	36	577.500	474.555
12	-577.500	-553.370	37	577.500	549.555
13	-288.990	-576.500	38	301.020	576.500
14	-213.990	-576.500	39	226.020	576.500
15	-138.990	-576.500	40	151.020	576.500
16	-63.990	-576.500	41	76.020	576.500
17	11.010	-576.500	42	1.020	576.500

Pad No.	X	Y	Pad No.	X	Y
18	86.010	-576.500	43	-73.980	576.500
19	161.010	-576.500	44	-148.980	576.500
20	236.010	-576.500	45	-223.980	576.500
21	311.010	-576.500	46	-298.980	576.500
22	374.110	-358.830	47	-373.980	576.500
23	577.500	-546.960	48	-448.980	576.500
24	577.500	-471.960	49	-523.980	576.500
25	577.500	-350.445			

Pad Assignment for COG

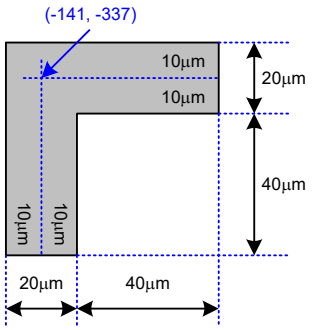
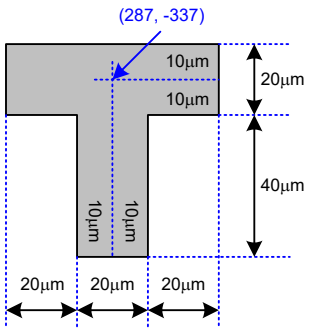


* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Dimensions for COG

Item	Pad Number.	Size		Unit
		X	Y	
Chip size	—	1328	1326	μm
Chip thickness	—	508		μm
Pad pitch	All Pad	≥75		μm
Bump size	1~12, 24~38	54	44	μm
	13,15~22,39~50	44	54	μm
Bump Spacing	All pad	≥21		μm
Bump height	All pad	18±3		μm

Alignment Mark Dimensions for COG

Item	Number	Size	Unit
ALIGN_A	14		μm
ALIGN_B	23		μm

Pad Coordinates for COG

Unit: μm

No	Name	X	Y	No	Name	X	Y
1	SEG1	-513.000	300.780	26	SEG26	575.000	-350.445
2	SEG0	-513.000	225.780	27	SEG25	575.000	-275.445
3	$\overline{CS}$	-513.000	150.780	28	SEG24	575.000	-200.445
4	$\overline{RD}$	-513.000	75.780	29	SEG23	575.000	-125.445
5	$\overline{WR}$	-513.000	0.780	30	SEG22	575.000	-50.445
6	DATA	-513.000	-74.220	31	SEG21	575.000	24.555
7	VSS	-513.000	-149.220	32	SEG20	575.000	99.555
8	OSCO	-513.000	-224.220	33	SEG19	575.000	174.555

No	Name	X	Y	No	Name	X	Y
9	OSCI	-513.000	-299.220	34	SEG18	575.000	249.555
10	VLCD	-513.000	-374.220	35	SEG17	575.000	324.555
11	VDD	-513.000	-457.465	36	SEG16	575.000	399.555
12	$\overline{IRQ}$	-513.000	-553.370	37	SEG15	575.000	474.555
13	BZ	-288.990	-574.000	38	SEG14	575.000	549.555
14	ALIGN_A	-141.000	-337.000	39	SEG13	301.020	574.000
15	$\overline{BZ}$	-213.990	-574.000	40	SEG12	226.020	574.000
16	COM0	-138.990	-574.000	41	SEG11	151.020	574.000
17	COM1	-63.990	-574.000	42	SEG10	76.020	574.000
18	COM2	11.010	-574.000	43	SEG9	1.020	574.000
19	COM3	86.010	-574.000	44	SEG8	-73.980	574.000
20	SEG31	161.010	-574.000	45	SEG7	-148.980	574.000
21	SEG30	236.010	-574.000	46	SEG6	-223.980	574.000
22	SEG29	311.010	-574.000	47	SEG5	-298.980	574.000
23	ALIGN_B	287.000	-337.000	48	SEG4	-373.980	574.000
24	SEG28	575.000	-546.960	49	SEG3	-448.980	574.000
25	SEG27	575.000	-471.960	50	SEG2	-523.980	574.000

Pad Description

Pad No.	Pad Name	I/O	Function
2, 1, 49~19	SEG0~SEG31	O	LCD segment outputs
3	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the HT1621S are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1621S are all enabled.
4	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the HT1621S are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
5	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the HT1621S on the rising edge of the $\overline{WR}$ signal.
6	DATA	I/O	Serial data input/output with pull-high resistor
7	VSS	—	Negative power supply, ground
9	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
8	OSCO	O	
10	VLCD	I	LCD power input
11	VDD	—	Positive power supply
12	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
13, 14	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
15~18	COM0~COM3	O	LCD common outputs

Absolute Maximum Ratings

Supply Voltage.....V_{SS}–0.3V to V_{SS}+6.5V

Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature.....–55°C to 150°C

Operating Temperature.....–40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	300	μA
		5V		—	300	600	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	60	120	μA
		5V		—	120	240	μA
I_{DD3}	Operating Current	3V	No load/LCD ON External clock source	—	100	200	μA
		5V		—	200	400	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	0.1	1.0	μA
		5V		—	0.3	2.0	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	6	—	—	mA
		5V	V_{OL}=0.5V	12	—	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	-6	—	—	mA
		5V	V_{OH}=4.5V	-12	—	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	250	400	—	μA
		5V	V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{OH}=4.5V	-300	-500	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	250	400	—	μA
		5V	V_{OL}=0.5V	500	800	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{OH}=4.5V	-300	-500	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	100	170	kΩ
		5V		20	50	90	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	28.8	32.0	35.2	kHz
f_{SYS2}	System Clock	—	Crystal oscillator	—	32768	—	Hz
f_{SYS3}	System Clock	—	External clock source	—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	$f_{SYS1}/128$	—	Hz
		—	Crystal oscillator	—	$f_{SYS2}/128$	—	Hz
		—	External clock source	—	$f_{SYS3}/1024$	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	—	—	1000	kHz
		5V		—	—	2000	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	500	kHz
		5V		—	—	1000	kHz
f_{TONE}	Tone Frequency (2kHz)	3V	On-chip RC oscillator	1.5	2.0	2.5	kHz
	Tone Frequency (4kHz)			3.0	4.0	5.0	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	250	300	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	0.50	—	—	μs
			Read mode	1.00	—	—	
		5V	Write mode	0.25	—	—	μs
			Read mode	0.50	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	C_O=15pF	—	50	100	ns
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	50	100	—	ns
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	100	200	—	ns
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	200	300	—	ns
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	100	200	—	ns
t_{PD}	DATA Output Delay Time ($\overline{RD}$ Falling to DATA)	—	C_O=15pF t_{PD}=50% to 50%	—	100	200	ns
t_{OFF}	V_{DD} OFF Time (Figure 4)	—	V_{DD} drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Rising Slew Rate (Figure 4)	—	—	0.05	—	—	V/ms
t_{RSTD}	Delay Time after Reset (Figure 4)	—	—	1	—	—	ms

Note: 1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.

2. If the V_{DD} drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the V_{DD} must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

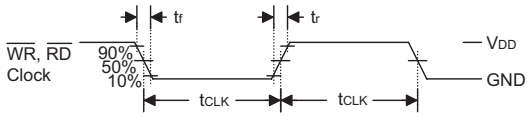


Figure 1

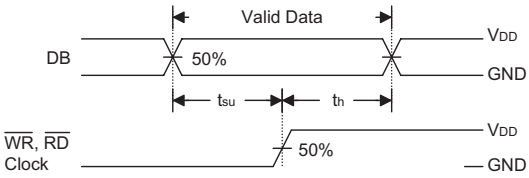


Figure 2

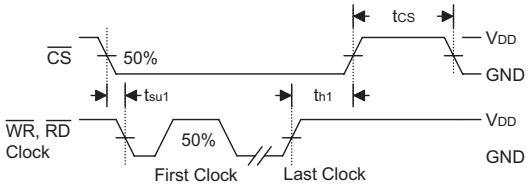


Figure 3

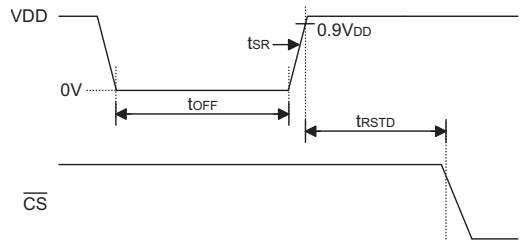
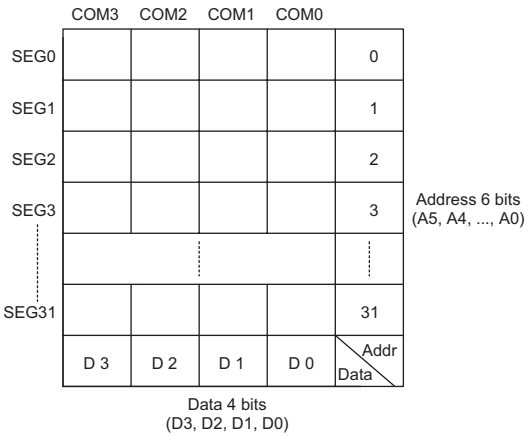


Figure 4 Power-on Reset Timing

Functional Description

Display Memory – RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



RAM Mapping

System Oscillator

The HT1621S system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the HT1621S is at the SYS DIS state.

Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

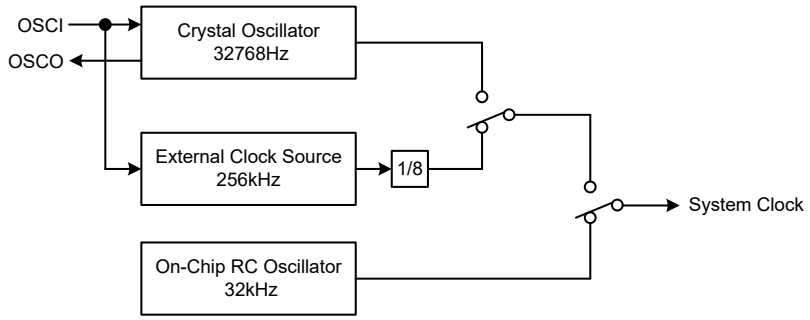
$$f_{WDT} = \frac{32kHz}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (32kHz), or an external frequency of 256kHz.

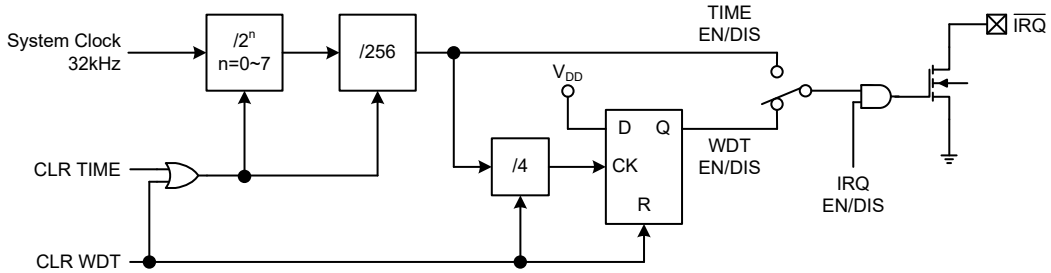
If an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or

the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/ WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the HT1621S will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.



System Oscillator Configuration



Timer and WDT Configurations

Tone Output

A simple tone generator is implemented in the HT1621S. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

LCD Driver

The HT1621S is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1621S suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. It is a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel

related commands. Using the LCD related commands, the HT1621S can be compatible with most types of LCD panels.

Name	Command Code	Function
LCD OFF	**1 0 0** 0 0 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	**1 0 0** 0 0 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	**1 0 0** 0 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

Command Format

The HT1621S can be configured by the S/W setting. There are two mode commands to configure the HT1621S resources and to transfer the LCD display data. The configuration mode of the HT1621S is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

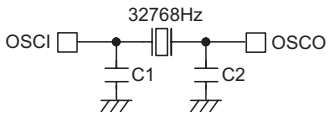
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0" a new operation mode ID should be issued first.

Interfacing

Only four lines are required to interface with the HT1621S. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1621S. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1621S are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1621S. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1621S on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1621S. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the HT1621S.

Crystal Selection

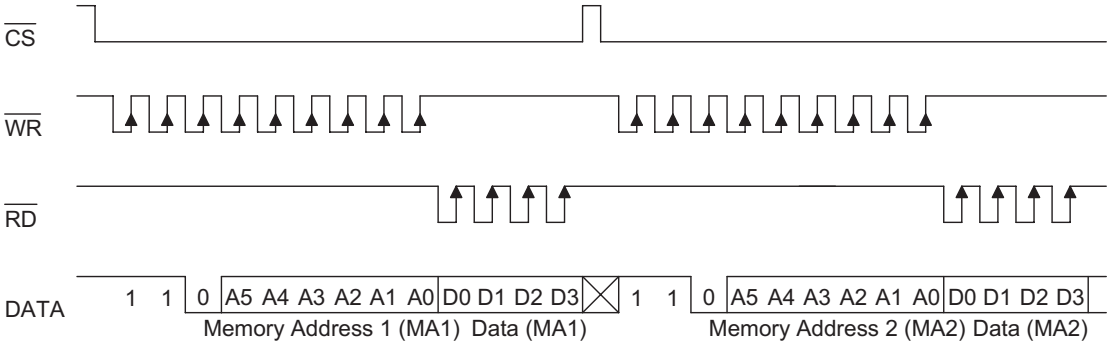
A 32768Hz crystal can be directly connected to the HT1621S via OSCI and OSCO. In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities. The table illustrates the suggestion value of capacities (C1, C2).



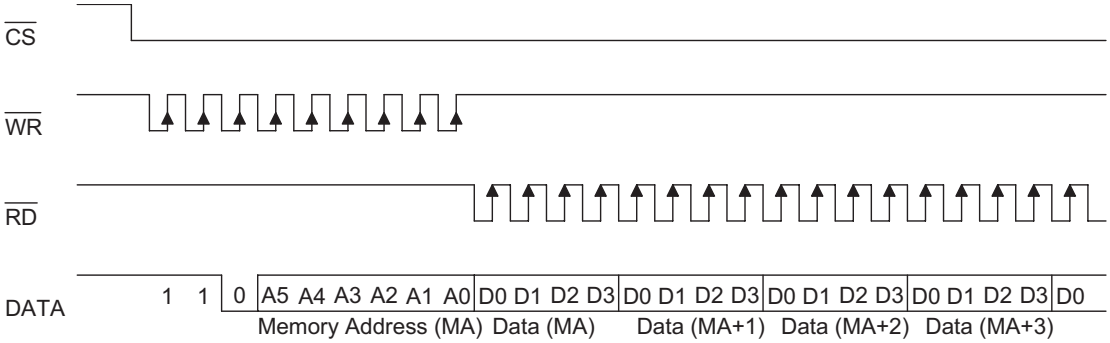
Crystal Error	Capacity Value
±10ppm	0~10p
10~20ppm	10~20p

Timing Diagrams

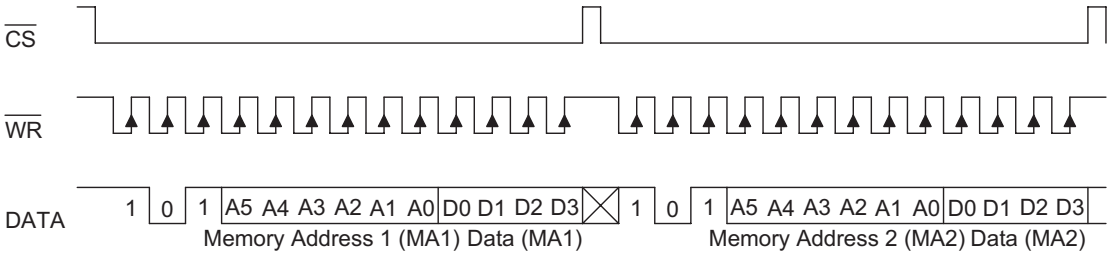
READ Mode (Command Code : 1 1 0)



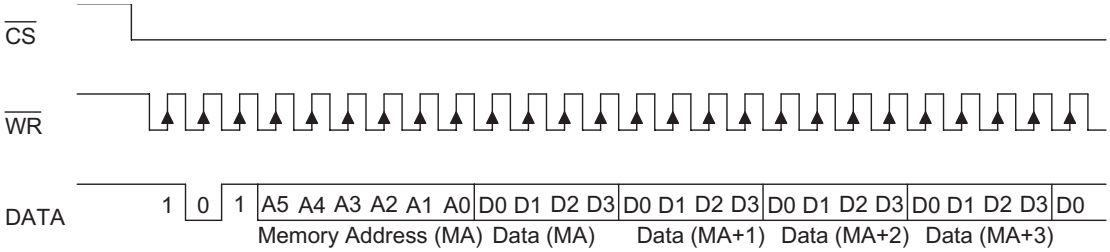
READ Mode (Successive Address Reading)



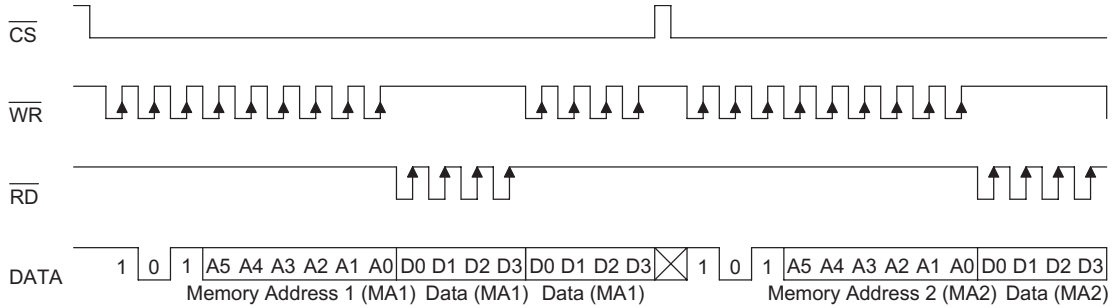
WRITE Mode (Command Code : 1 0 1)



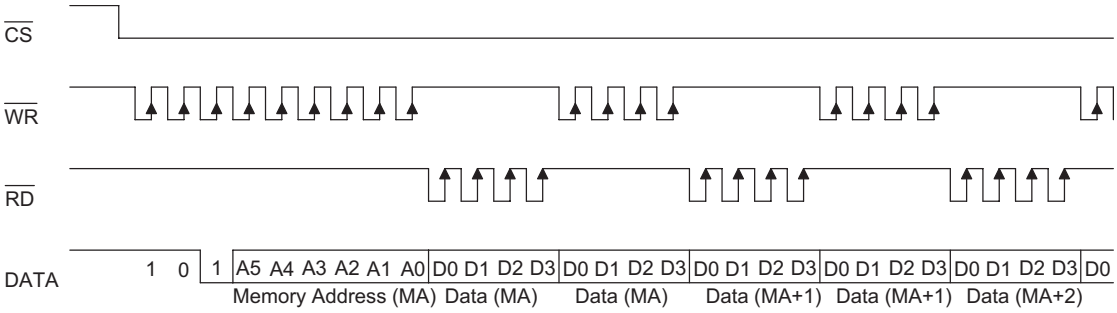
WRITE Mode (Successive Address Writing)



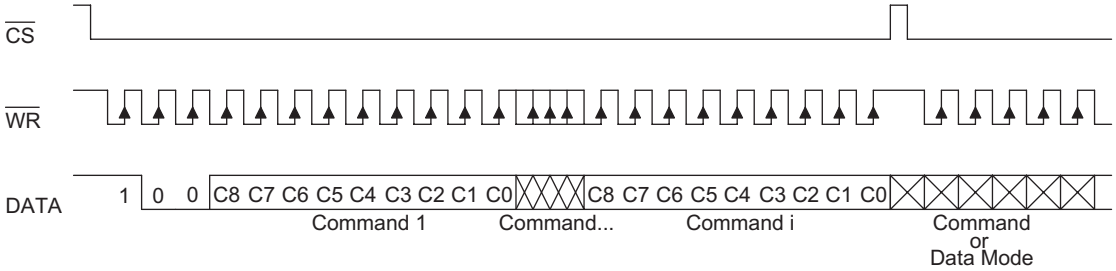
Read-Modify-Write Mode (Command Code : 1 0 1)



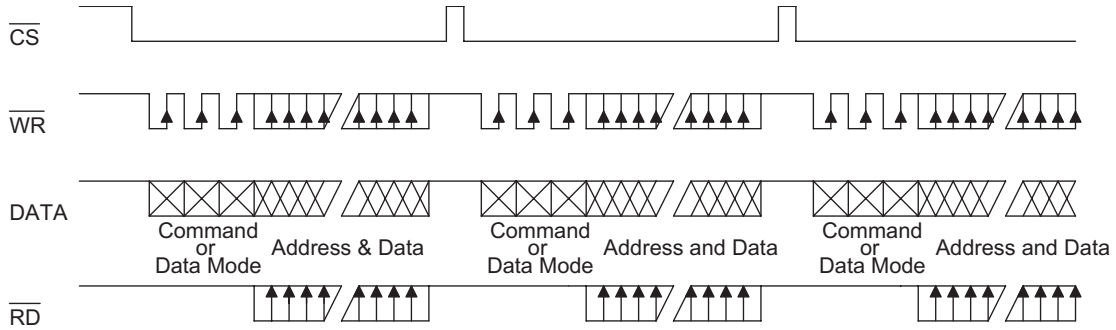
Read-Modify-Write Mode (Successive Address Accessing)



Command Mode (Command Code : 1 0 0)



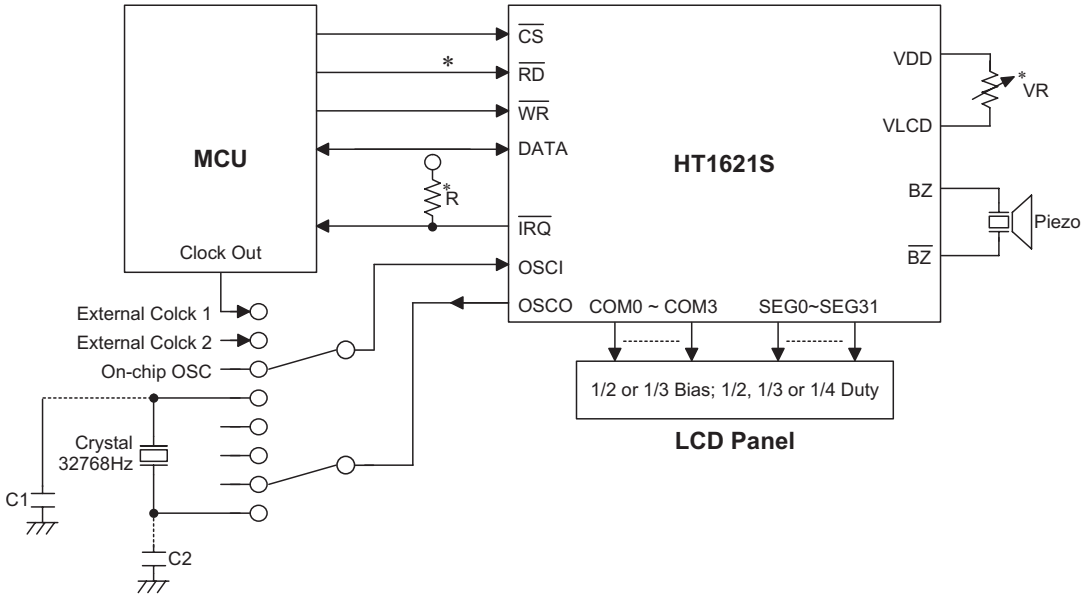
Mode (Data and Command Mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

Application Circuits

Host Controller with an HT1621S Display System



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.

The voltage applied to V_{LCD} pin must be equal to or lower than V_{DD}.

Adjust VR to fit user's LCD panel display voltage (V_{LCD})

Adjust R (external pull-high resistance) to fit user's time base clock.

In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities.

The table illustrates the suggestion value of capacities (C1,C2)

Crystal Error	Capacity Value
±10ppm	0~10p
10~20ppm	10~20p

Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	**1 1 0**	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	**1 0 1**	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**1 0 1**	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	**1 0 0**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	**1 0 0**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**1 0 0**	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	**1 0 0**	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	**1 0 0**	0000-0100-X	C	Disable time base output	
WDT DIS	**1 0 0**	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	**1 0 0**	0000-0110-X	C	Enable time base output	
WDT EN	**1 0 0**	0000-0111-X	C	Enable WDT time-out flag output	

Name	ID	Command Code	D/C	Function	Def.
TONE OFF	**1 0 0**	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	**1 0 0**	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	**1 0 0**	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	**1 0 0**	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	**1 0 0**	0001-01XX-X	C	System clock source, crystal oscillator	
RC 32K	**1 0 0**	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	**1 0 0**	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	**1 0 0**	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	**1 0 0**	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	**1 0 0**	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	**1 0 0**	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	**1 0 0**	100X-0XXX-X	C	Disable IRQ output	Yes
IRQ EN	**1 0 0**	100X-1XXX-X	C	Enable IRQ output	
F1	**1 0 0**	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	**1 0 0**	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	**1 0 0**	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	**1 0 0**	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	**1 0 0**	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	**1 0 0**	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	Yes
TEST	**1 0 0**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Note: X: Don't care

A5~A0: RAM addresses

D3~D0: RAM data

D/C: Data/command mode

Def.: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1621S after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1621S.

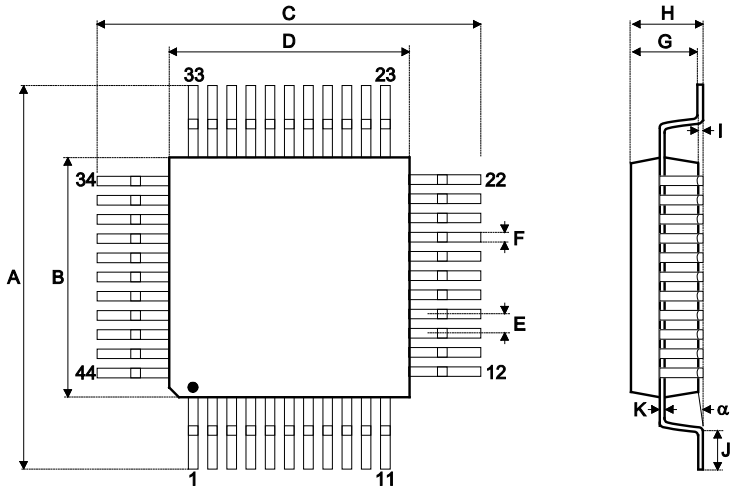
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

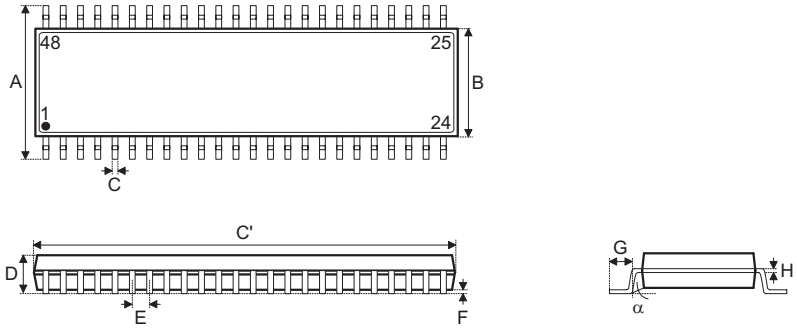
44-pin LQFP (10mm×10mm) (FP2.0mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.032 BSC	—
F	0.012	0.015	0.018
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12.00 BSC	—
B	—	10.00 BSC	—
C	—	12.00 BSC	—
D	—	10.00 BSC	—
E	—	0.80 BSC	—
F	0.30	0.37	0.45
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

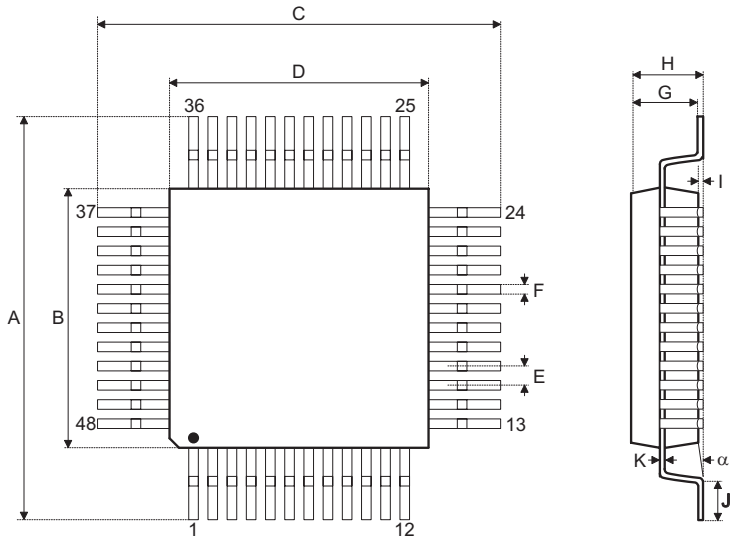
48-pin SSOP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.395	—	0.420
B	0.291	0.295	0.299
C	0.008	—	0.014
C’	0.620	0.625	0.630
D	0.095	0.102	0.110
E	—	0.025 BSC	—
F	0.008	0.012	0.016
G	0.020	—	0.040
H	0.005	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	10.03	—	10.67
B	7.39	7.49	7.59
C	0.20	—	0.34
C’	15.75	15.88	16.00
D	2.41	2.59	2.79
E	—	0.635 BSC	—
F	0.20	0.30	0.41
G	0.51	—	1.02
H	0.13	—	0.25
α	0°	—	8°

48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°