Features

- Operating voltage: 2.4V~5.5V
- Internal 32kHz RC oscillator
- Bias: 1/2 or 1/3; Duty: 1/4
- Internal LCD bias generation with voltage-follower buffers
- I^2C bus interface
- Two selectable LCD frame frequencies: 80Hz or 160Hz
- Up to 44×4 bits RAM for display data storage
- Max. 44×4 patterns: 44 segments and 4 commons
- Versatile blinking modes
- R/$\overline{W}$ address auto increment
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Low power consumption
- Provides the VLCD pin to adjust LCD operating voltage
- Manufactured in silicon gate CMOS process
- Package Types: 48/52-pin LQFP and COG

Applications

- Electronic meter
- Water meter
- Gas meter
- Heat energy meter
- Household appliance
- Games
- Telephone
- Consumer electronics

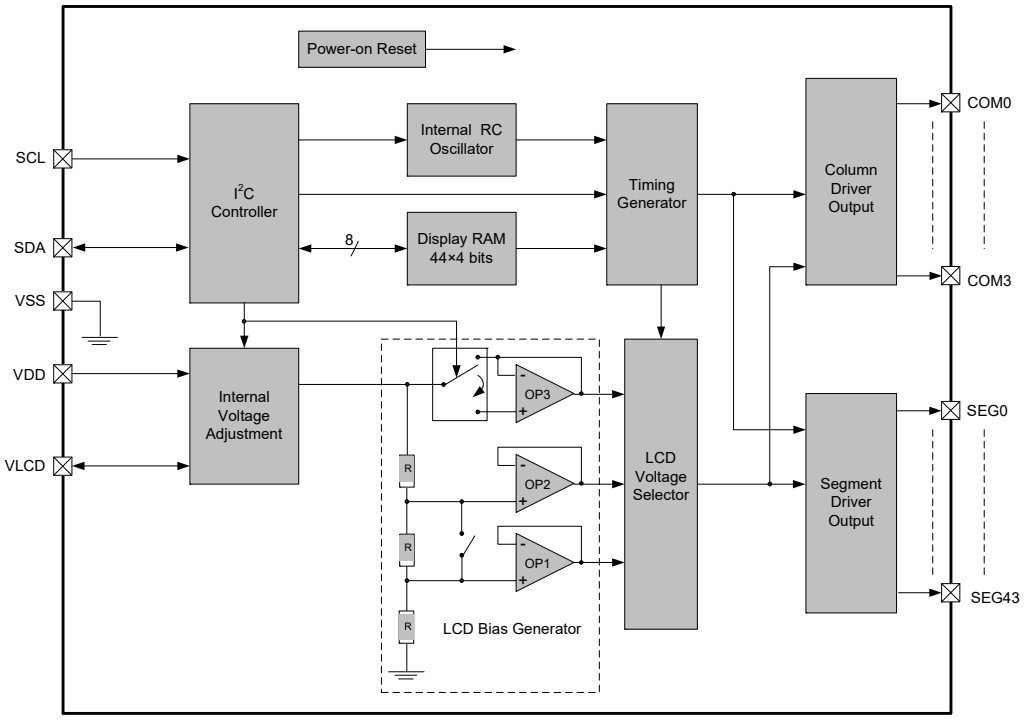
General Description

The HT16C22A/HT16C22AG devices are a memory mapping and multi-function LCD controller driver. The maximum display segments of the devices are 176 patterns (44 segments and 4 commons). The software configuration feature of the HT16C22A/HT16C22AG devices make it suitable for multiple LCD applications including LCD modules and display subsystems. The HT16C22A/HT16C22AG devices communicate with most microprocessors/microcontrollers via a two-line bidirectional I^2C bus.

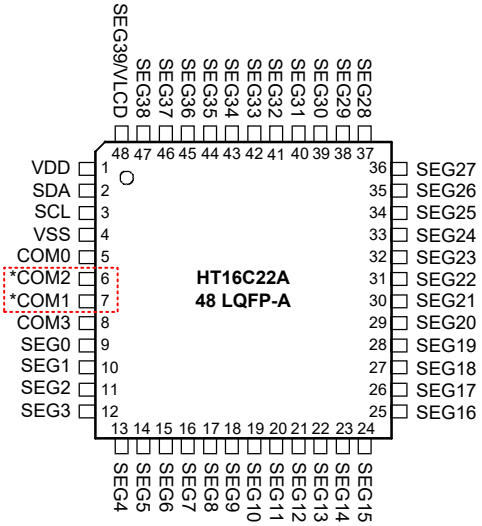
Selection Table

Part No.	VDD	Max. Resolution Segment × Common	LCD Voltage	Bias	Interface	Package
HT16C22A	2.4V~5.5V	44×4	≤ V_{DD}	1/2, 1/3	I^2C	48/52LQFP
HT16C22AG						Gold Bump

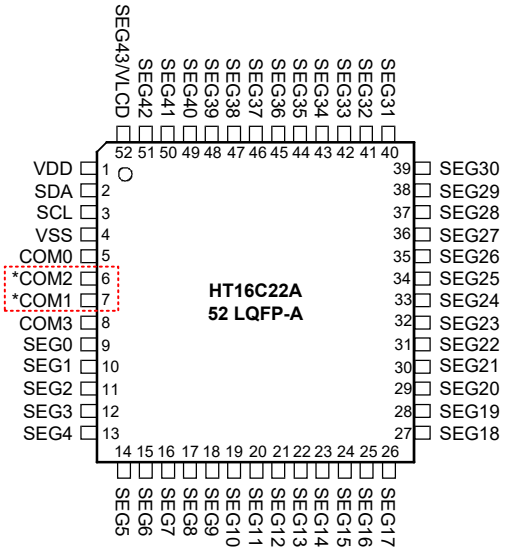
Block Diagram



Pin Assignment

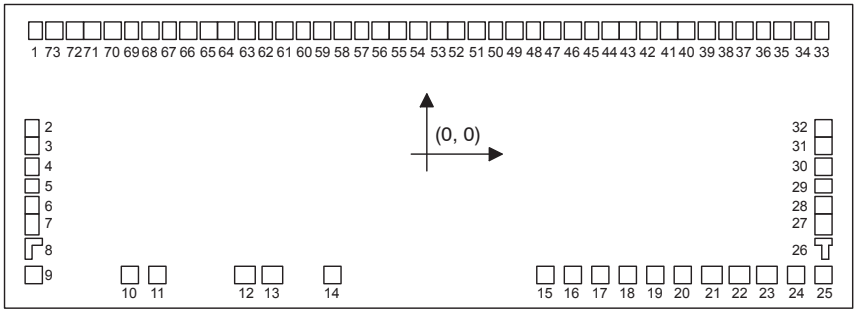


Note: The *COM1 and *COM2 pins are not in sequential order.



Note: The *COM1 and *COM2 pins are not in sequential order.

Pad Assignment for COG



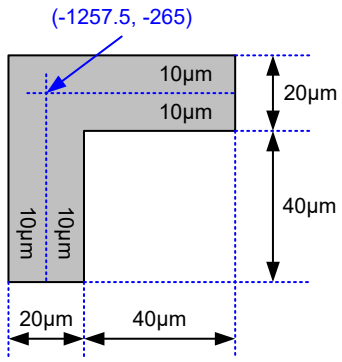
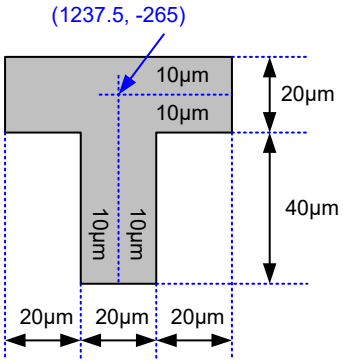
Note:

Internal Voltage Adjustment (IVA) Set Command		VLCD (PAD14)	Segment43 (PAD5)	Note
DE Bit	VE Bit			
0	0	Input	Null	The VLCD input voltage can be smaller than or equal to VDD
0	1	Output	Null	The VLCD pin is an output pin of which the voltage can be detected by the external MCU host.
1	0	Null	Output	—
1	1	Null	Output	—

Pad Dimensions for COG

Item	Number		Size		Unit
			X	Y	
Chip size	—		2656	938	μm
Chip thickness	—		508		μm
Pad pitch	1~7, 27~73		60		μm
	9~25		87		μm
Bump size	Output pad	34~73	40	60	μm
		2~5, 29~32	60	40	μm
	Input pad	10~14	67	67	μm
	Dummy pad	1, 33	40	60	μm
		6~7, 27~28	60	40	μm
		9, 15~25	67	67	μm
Bump height	All pad		18±3		μm

Alignment Mark Dimensions for COG

Item	Number	Size	Unit
ALIGN_A	8		μm
ALIGN_B	26		μm

Pad Coordinates for COG

Unit: μm

No	Name	X	Y	No	Name	X	Y
1	DUMMY	-1230	379 .5	39	SEG5	870	379.5
2	SEG40	-1238.5	86.25	40	SEG6	810	379.5
3	SEG41	-1238.5	26.25	41	SEG7	750	379.5
4	SEG42	-1238.5	-33.75	42	SEG8	690	379.5
5	SEG43	-1238.5	-93.75	43	SEG9	630	379.5
6	DUMMY	-1238.5	-153.75	44	SEG10	570	379.5
7	DUMMY	-1238.5	-213.75	45	SEG11	510	379.5
9	DUMMY	-1235	-370.4	46	SEG12	450	379.5
10	SDA	-933	-370.4	47	SEG13	390	379.5
11	SCL	-846	-370.4	48	SEG14	330	379.5
12	VDD	-575	-370.4	49	SEG15	270	379.5
13	VSS	-488	-370.4	50	SEG16	210	379.5
14	VLCD	-300	-370.4	51	SEG17	150	379.5
15	DUMMY	365	-370.4	52	SEG18	90	379.5
16	DUMMY	452	-370.4	53	SEG19	30	379.5
17	DUMMY	539	-370.4	54	SEG20	-30	379.5
18	DUMMY	626	-370.4	55	SEG21	-90	379.5
19	DUMMY	713	-370.4	56	SEG22	-150	379.5
20	DUMMY	800	-370.4	57	SEG23	-210	379.5
21	DUMMY	887	-370.4	58	SEG24	-270	379.5
22	DUMMY	974	-370.4	59	SEG25	-330	379.5
23	DUMMY	1061	-370.4	60	SEG26	-390	379.5
24	DUMMY	1148	-370.4	61	SEG27	-450	379.5
25	DUMMY	1235	-370.4	62	SEG28	-510	379.5
27	DUMMY	1238.5	-213.75	63	SEG29	-570	379.5
28	DUMMY	1238.5	-153.75	64	SEG30	-630	379.5
29	COM0	1238.5	-93.75	65	SEG31	-690	379.5
30	COM1	1238.5	-33.75	66	SEG32	-750	379.5
31	COM2	1238.5	26.25	67	SEG33	-810	379.5
32	COM3	1238.5	86.25	68	SEG34	-870	379.5
33	DUMMY	1230	379.5	69	SEG35	-930	379.5
34	SEG0	1170	379.5	70	SEG36	-990	379.5
35	SEG1	1110	379.5	71	SEG37	-1050	379.5
36	SEG2	1050	379.5	72	SEG38	-1110	379.5
37	SEG3	990	379.5	73	SEG39	-1170	379.5
38	SEG4	930	379.5				

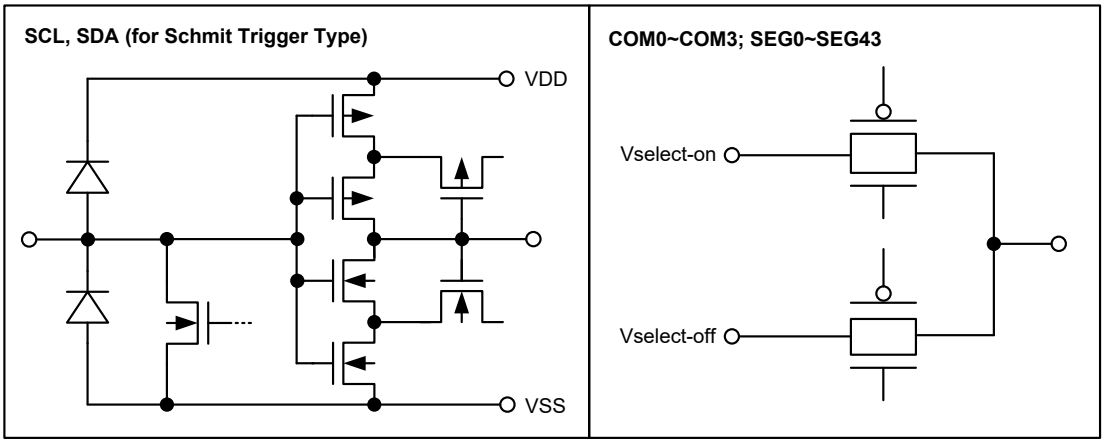
Alignment Mark Coordinates for COG

No	Name	X	Y	No	Name	X	Y
8	ALIGN_A	-1257.5	-265	26	ALIGN_B	1237.5	-265

Pin Description

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output for I^2C interface
SCL	I	Serial Clock Input for I^2C interface
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
VLCD	—	Power supply for LCD driver • One external resistor is connected between the VLCD pin and the VDD pin to determine the bias voltage for packages with a VLCD pin. Internal voltage adjustment function is disabled. • Internal voltage adjustment function can be used to adjust the V_{LCD} voltage. If the VLCD pin is used as voltage detection pin, an external power supply should not be applied to the VLCD pin. • An external MCU can detect the voltage of the VLCD pin and program the internal voltage adjustment for packages with a VLCD pin.
COM0~COM3	O	LCD Common outputs
SEG0~SEG43	O	LCD Segment outputs

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}−0.3V to V_{SS}+6.5V

Input Voltage ..... V_{SS}−0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, V_{LCD}=2.4V~5.5V, Ta=−40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	Operating Voltage	—	—	2.4	—	V_{DD}	V
I_{DD}	Operating Current	3V	No load, V_{LCD}=V_{DD}, 1/3 bias, f_{LCD}=80Hz, LCD display on, internal system oscillator on, DA0~DA3 are set to "0000"	—	18	27	μA
		5V		—	25	40	μA
		3V	No load, V_{LCD}=V_{DD}, 1/3 bias f_{LCD}=80Hz, LCD display off, internal system oscillator on, DA0~DA3 are set to "0000"	—	2	5	μA
		5V		—	4	10	μA
I_{STB}	Standby Current	3V	No load, V_{LCD}=V_{DD}, LCD display off, internal system oscillator off	—	—	1	μA
		5V		—	—	2	μA
V_{IH}	Input High Voltage	—	SDA, SCL	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	SDA, SCL	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low Level Output Current	3V	V_{OL}=0.4V on SDA pin	3	—	—	mA
		5V		6	—	—	mA
I_{OL1}	LCD Common Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH1}	LCD Common Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA
I_{OL2}	LCD Segment Sink Current	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	—	μA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD Segment Source Current	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	—	μA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA

A.C. Characteristics

V_{SS}=0V, V_{DD}=2.4V~5.5V, V_{LCD}=2.4V~5.5V, Ta=−40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{LCD1}	LCD Frame Frequency	4V	1/4 duty, Ta=25°C	72	80	88	Hz
		4V	1/4 duty, Ta=-40°C~+85°C	52	80	124	Hz
f_{LCD2}	LCD Frame Frequency	4V	1/4 duty, Ta=25°C	144	160	176	Hz
		4V	1/4 duty, Ta=-40°C~+85°C	104	160	248	Hz
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{VDD}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to Remain at V_{POR} to Ensure Power-on Reset	—	—	10	—	—	ms

I²C Interface A.C. Characteristics

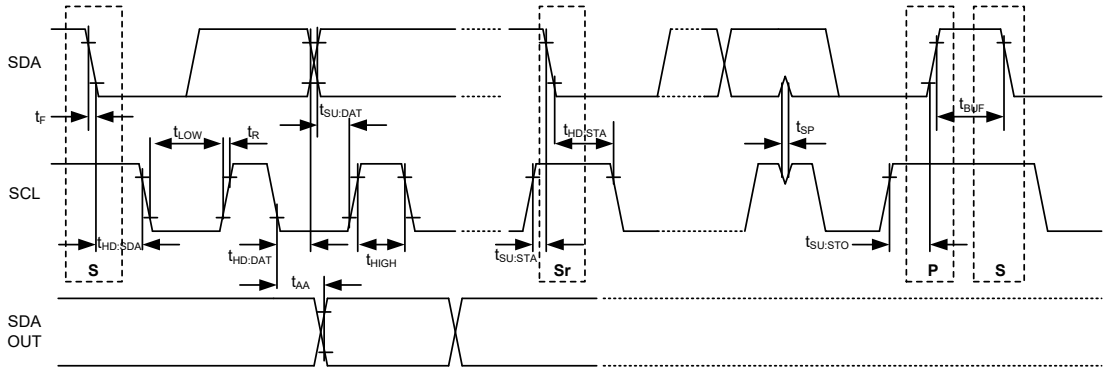
Ta=−40°C~85°C

Symbol	Parameter	Conditions	V_{DD}=2.4V~5.5V		V_{DD}=3.0V~5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock Frequency	—	—	100	—	400	kHz
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD:STA}$	Start Condition Hold Time	After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t_{LOW}	SCL Low Time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High Time	—	4.0	—	0.6	—	μs
$t_{SU:STA}$	Start Condition Setup Time	Only relevant for repeated START condition	4.7	—	0.6	—	μs
$t_{HD:DAT}$	Data Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Setup Time	—	250	—	100	—	ns
t_R	SDA and SCL Rising Fime(Note)	—	—	1.0	—	0.3	μs
t_F	SDA and SCL Falling Time(Note)	—	—	0.3	—	0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time	—	4.0	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

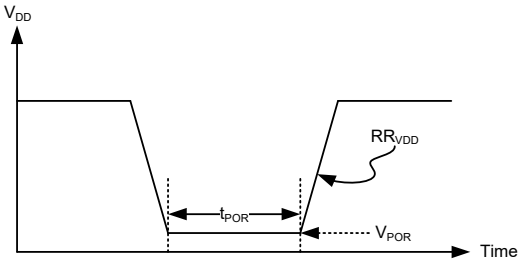
Timing Diagrams

I²C Timing



Power-on Reset Timing

The devices must be powered up under certain conditions to ensure correct operation as shown in the accompanying diagram.



Note that if the power-on reset timing conditions are not satisfied during the Power-on/off sequence, the internal power-on reset circuit will not operate normally. Also if V_{DD} drops below the minimum voltage of operating voltage specification during operation, the power-on reset timing conditions must be also satisfied. This means that V_{DD} must fall to 0V and remain at 0V for a minimum time of 10ms before rising to the normal operating voltage.

Functional Description

Power-on Reset

When power is applied, the devices are initialised by an internal power-on reset circuit. The status of the internal circuits after initialisation is as follows:

- All common outputs are set to V_{DD}
- All segment outputs are set to V_{DD}
- The drive mode 1/4 duty output and 1/3 bias is selected
- The System Oscillator and the LCD bias generator are both off
- LCD Display is off
- Internal voltage adjustment function is enabled
- Detection switch for VLCD pin is disabled
- Frame Frequency is set to 80Hz
- Blinking function is switched off

Data transfers on the I²C bus should be avoided for 1ms following power-on to allow completion of the reset action.

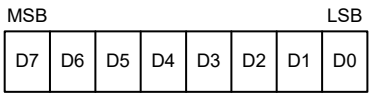
Display Memory − RAM Structure

The display RAM is a static 44×4 bits RAM which stores LCD data. Logic “1” in the RAM bit-map indicates the “on” state of the corresponding LCD segment; similarly logic “0” indicates the “off” state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the 44 segments operated with respect to COM0. In multiplexed LCD applications the segment data of the second, third and fourth columns of the display RAM are time-multiplexed with COM1, COM2 and COM3 respectively. The following is a mapping from the RAM data to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
:	:	:	:	:	:	:	:	:	:	:
SEG43					SEG42					15H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

Display data transfer format for the I²C bus:



System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The system clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power-on the system oscillator will be in the stop state.

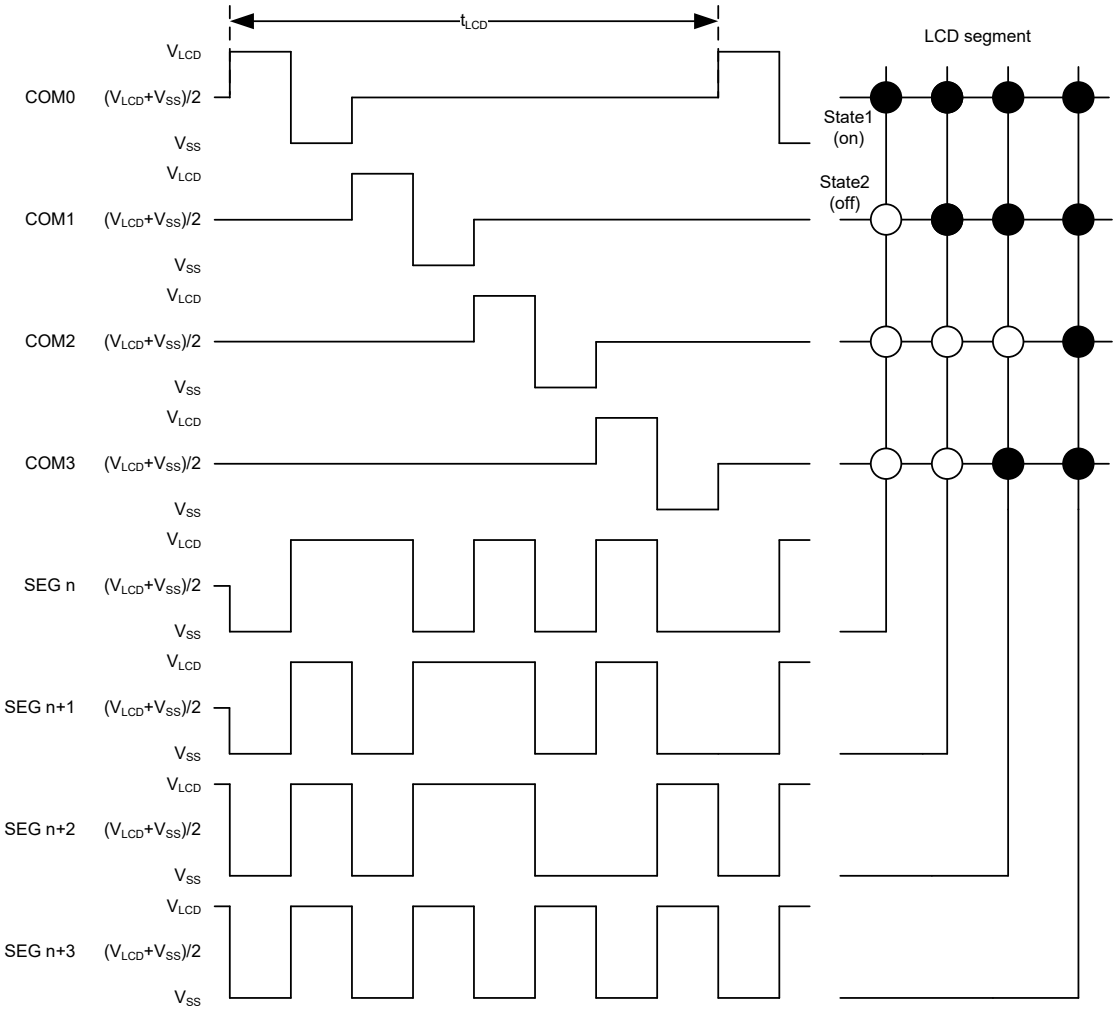
LCD Bias Generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{LCD} – V_{SS}$. The LCD voltage may be temperature compensated externally through the voltage supply to the VLCD pin.

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between the VLCD and VSS pins. The centre resistor can be switched out of the circuits to provide a 1/2 bias voltage level for the 1/4 duty configuration.

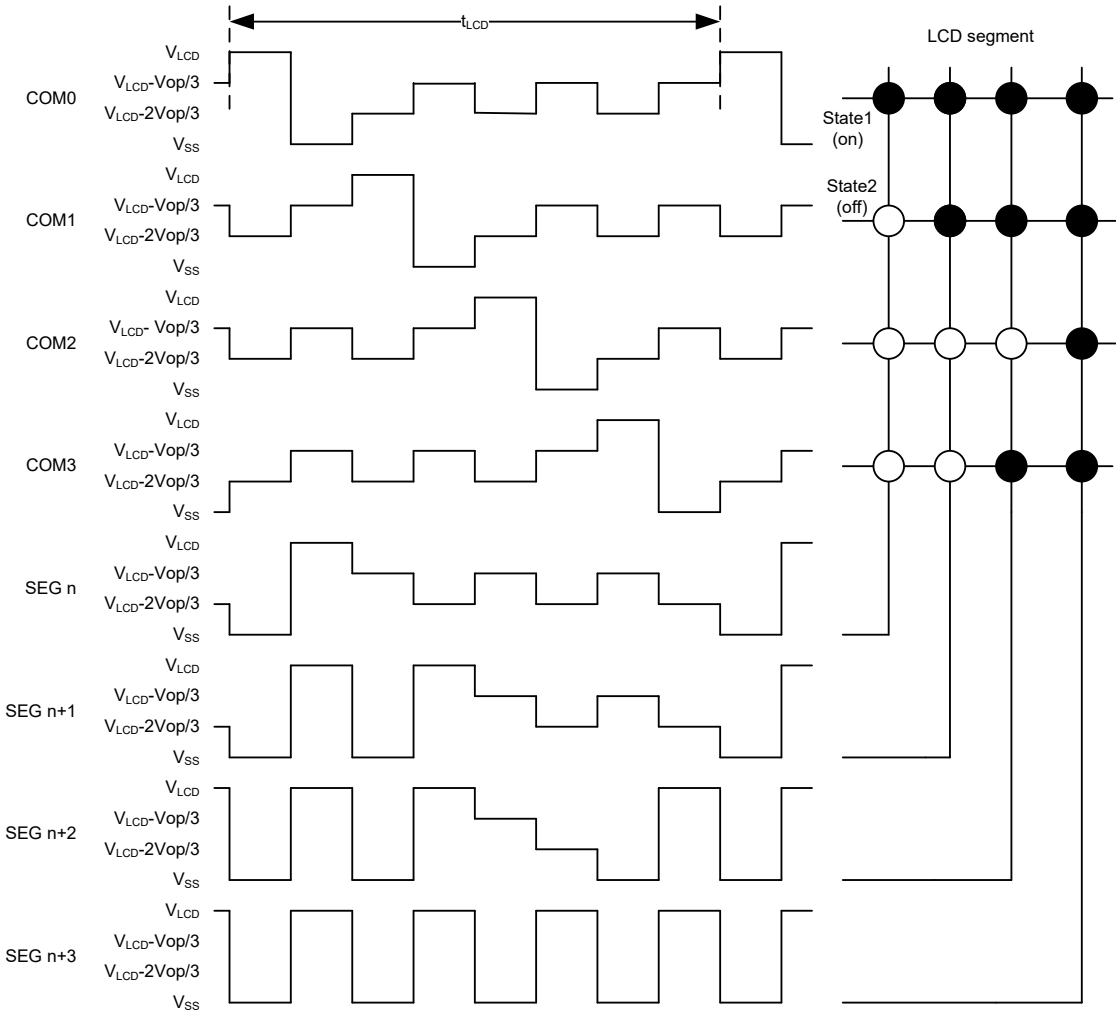
LCD Drive Mode Waveforms

When four columns are provided in the LCD, the 1/4 duty drive mode applies. The HT16C22A/HT16C22AG can use 1/2 or 1/3 bias type in output waveforms as shown as follows:



Note: $t_{LCD}=1/f_{LCD}$

Waveforms for 1/4 Duty Drive Mode with 1/2 Bias ($V_{OP}=V_{LCD}-V_{SS}$)



Note: $t_{LCD}=1/f_{LCD}$

Waveforms for 1/4 Duty Drive Mode with 1/3 Bias ($V_{OP}=V_{LCD}-V_{SS}$)

Segment Driver Outputs

The LCD drive section includes 44 segment outputs, SEG0~SEG43, which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. When less than 44 segment outputs are required the unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes 4 column outputs, COM0~COM3, which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. When less than 4 column outputs are required the unused column outputs should be left open-circuit.

Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer by the address pointer command.

Blinker Function

The devices contain versatile blinking capabilities. The whole display can be blinked at a frequency selected by the Blink command. The blinking frequency is a subdivided ratio of the system frequency. The ratio between the system oscillator and blinking frequency depends on the blinking mode in which the devices are operating, as shown in the table:

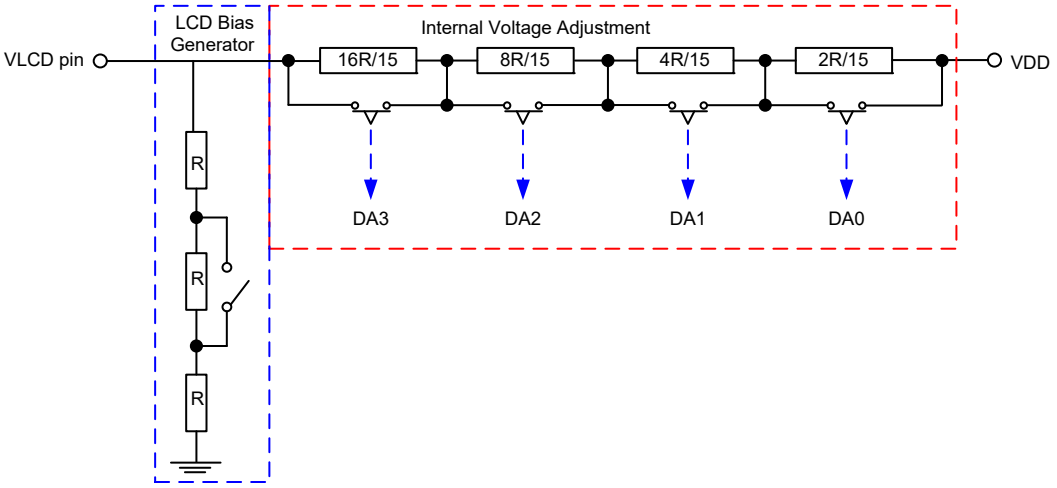
Blinking Mode	Operating Mode Ratio	Blinking Frequency (Hz)
0	0	Blink off
1	f_{SYS} / 16384	2
2	f_{SYS} / 32768	1
3	f_{SYS} / 65536	0.5

Frame Frequency

The HT16C22A/HT16C22AG provide two frame frequencies selected with the Mode Setting command: 80Hz and 160Hz.

V_{LCD} Voltage Adjustment

- The internal V_{LCD} adjustment contains four resistors in series and a 4-bit programmable analog switch which can provide sixteen voltage adjustment options using the V_{LCD} voltage adjustment command.
- The V_{LCD} adjustment structure is show in the diagram:



- The relationship between the programmable 4-bit analog switch and the V_{LCD} output voltage is shown in the table:

Bias / DA3~DA0	1/2	1/3	Note
00H	1.000×V_{DD}	1.000×V_{DD}	Default value
01H	0.9375×V_{DD}	0.957×V_{DD}	—
02H	0.882×V_{DD}	0.918×V_{DD}	—
03H	0.833×V_{DD}	0.882×V_{DD}	—
04H	0.789×V_{DD}	0.849×V_{DD}	—
05H	0.750×V_{DD}	0.818×V_{DD}	—
06H	0.714×V_{DD}	0.789×V_{DD}	—
07H	0.682×V_{DD}	0.763×V_{DD}	—
08H	0.652×V_{DD}	0.738×V_{DD}	—
09H	0.625×V_{DD}	0.714×V_{DD}	—

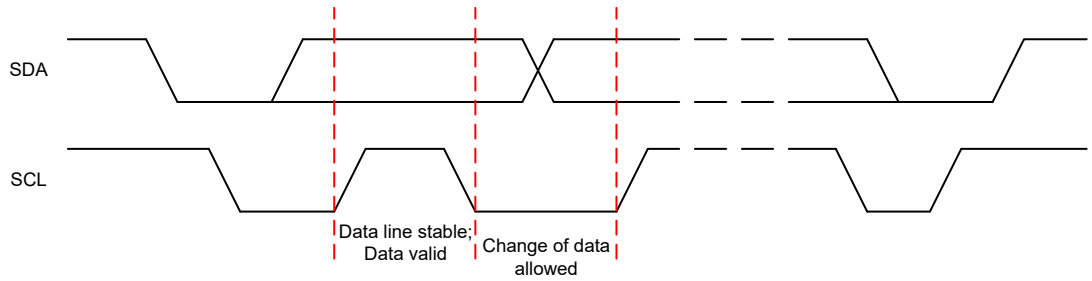
Bias / DA3~DA0	1/2	1/3	Note
0AH	0.600×V_{DD}	0.692×V_{DD}	—
0BH	0.577×V_{DD}	0.672×V_{DD}	—
0CH	0.556×V_{DD}	0.652×V_{DD}	—
0DH	0.536×V_{DD}	0.634×V_{DD}	—
0EH	0.517×V_{DD}	0.616×V_{DD}	—
0FH	0.500×V_{DD}	0.600×V_{DD}	—

I²C Serial Interface

The devices include an I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7kΩ. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

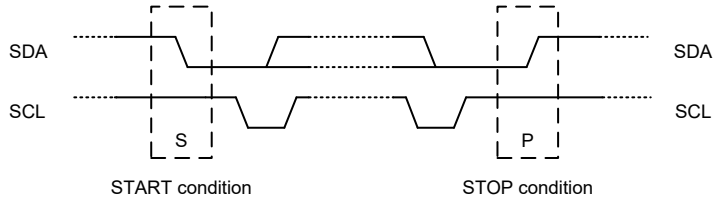
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only be changed when the clock signal on the SCL line is low as shown in the diagram.



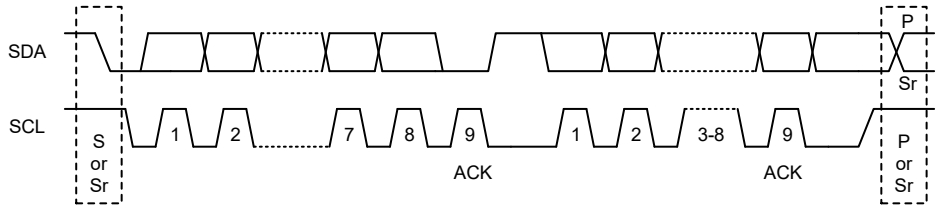
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START (S) and repeated START (Sr) conditions are functionally identical.



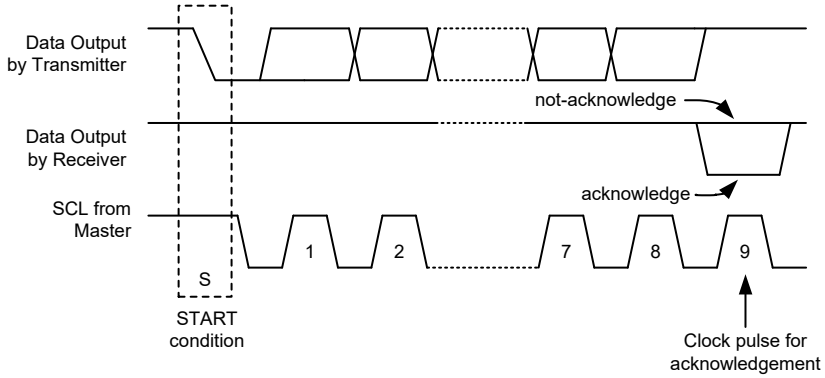
Byte Format

Every byte placed on the SDA line must be 8-bit in length. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



Acknowledge

- Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge bit, ACK, after the reception of each byte.
- The devices that acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



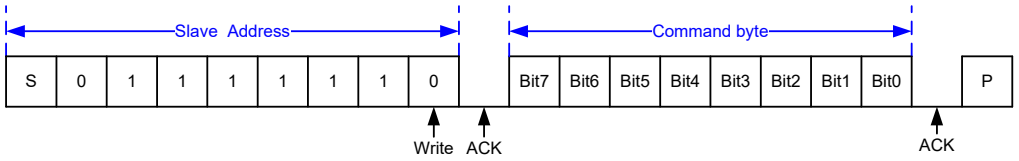
Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", a read operation is selected. A "0" selects a write operation.
- The HT16C22A/HT16C22AG address bits are "0111111". When an address byte is sent, the devices compare the first seven bits after the START condition. If they match, the devices output an acknowledge on the SDA line.

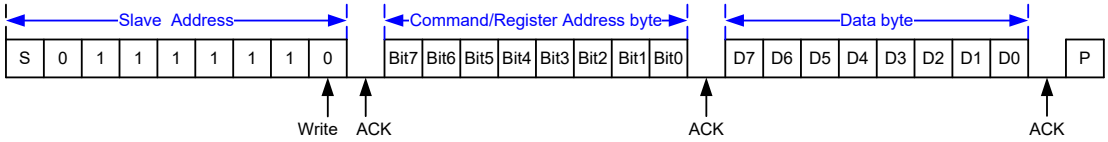
Write Operation

Byte Write Operation

A byte write operation requires a START condition, a slave address with an R/$\overline{W}$ bit, a valid Register Address, Data and a STOP condition. After each of the three bytes, the devices respond with an ACK.



Command Byte Received

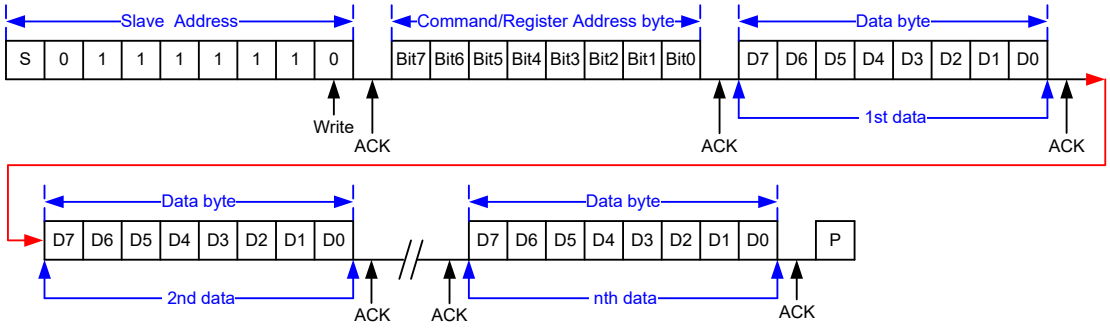


Single Data Byte Received

Note: If the byte following the slave address is a command code, the byte following the command code will be ignored.

Page Write Operation

After a START condition the slave address with the R/$\overline{W}$ bit is placed on the bus followed with the Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the internal address pointer will be increased by 1 to indicate the next memory address location after the reception of an acknowledge clock. After the internal address pointer reaches the maximum memory address, which is 15H, the address pointer will be reset to 00H.

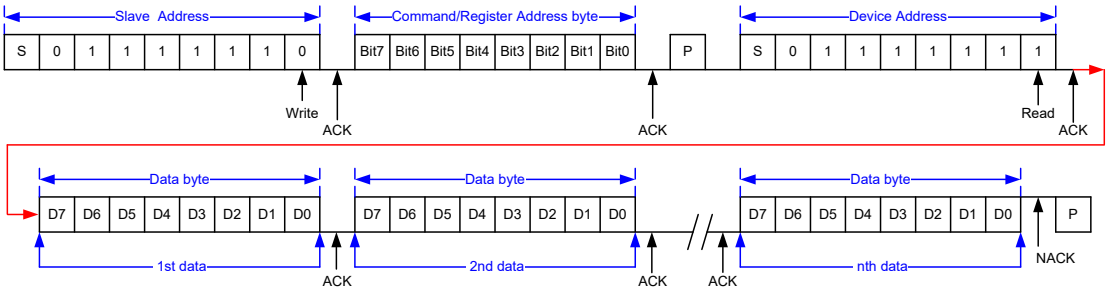


N Data Bytes Received

Read Operation

In this mode, the master reads the HT16C22A/HT16C22AG data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit and the Register Address (A_N) which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address are transferred on the bus followed by the R/$\overline{W}$ bit ="1"). Then the MSB of the data which was addressed is transmitted first on the I^2C bus. The address pointer is only increased by 1 after the reception of an acknowledge clock. That means that if the devices are configured to transmit the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the internal address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum memory address which is 15H, the pointer will be reset to 00H.

This cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Reading N Data Bytes

Command Summary

LCD Driver Setting Command

This command is used to set the frame frequency output and internal system oscillator on/off and display on/off and driver mode.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	Def
Mode Setting	1	0	0	F	S	E	0	M0		80H

Note: 1. When "M0" is set to "0":
The driver mode is set to 1/3 bias.
2. When "M0" is set to "1":
The driver mode is set to 1/2 bias.
3. When "S" and "E" bits are set to {0, X}:
Disable Internal System oscillator and display off.
4. When "S" and "E" bits are set to {1, 0}:
Enable Internal System oscillator and display off.
5. When "S" and "E" bits are set to {1, 1}:
Enable Internal System oscillator and display on.
6. When "F" bits is set to "0":
Frame Frequency=80Hz
7. When "F" bits is set to "1":
Frame Frequency=160Hz
8. Power-on status:
The drive mode 1/3 bias is selected.
Disable Internal System oscillator and display off.
Frame frequency is set to 80Hz.
9. If the programmed command data is not defined, the function will not be affected.

Display Data Input Setting Command

This command is used to send data from MCU to memory map of HT16C22A/HT16C22AG.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	Def
Address Pointer	0	0	0	A4	A3	A2	A1	A0	Display data start address of memory map	00H

Note: 1. Power-on status: the address is set to 00H.
2. After reaching the memory location 15H, the pointer will reset to 00H.
3. If the programmed command data is not defined, the function will not be affected.

Blinking Setting Command

This command is used to set the LCD blinking frequency of display modes.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	Def
Blinking Frequency	1	1	0	0	0	0	BK1	BK0		C0H

Note: 1. When "BK1" and "BK0" bits are set to {0, 0}:
Blinking off
2. When "BK1" and "BK0" bits are set to {0, 1}:
Blinking Frequency = 2Hz
3. When "BK1" and "BK0" bits are set to {1, 0}:
Blinking Frequency = 1Hz
4. When "BK1" and "BK0" bits are set to {1, 1}:
Blinking Frequency = 0.5Hz
5. Power-on status: Blinking is switched off.
6. If the programmed command data is not defined, the function will not be affected.

Internal Voltage Adjustment (IVA) Setting Command

The internal voltage (V_{LCD}) adjustment can provide sixteen kinds of regulator voltage adjustment options by setting LCD operating voltage adjustment command code.

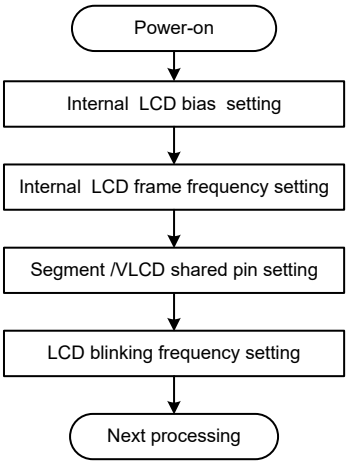
Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	Def
Internal Voltage Adjust Control	0	1	DE	VE	DA3	DA2	DA1	DA0	The Segment/VLCD shared pin can be programmed via the "DE" bit. The "VE" bit is used to enable or disable the internal voltage adjustment for bias voltage. DA3~DA0 can be used to adjust the V_{LCD} output voltage.	70H

Note: 1. When "DE" and "VE" bits are set to {0, 0}:
The Segment/VLCD shared pin is set as the VLCD pin.
Disable the internal voltage adjustment.
One external resister must be connected between the VLCD pin and VDD pin to determine the bias voltage, and the internal voltage follower (OP3) must be enabled by setting DA3~DA0 to a value other than "0000". If the VLCD pin is connected to the VDD pin, the internal voltage follower (OP3) must be disabled by setting DA3~DA0 to "0000".
2. When "DE" and "VE" bits are set to {0,1}:
The Segment/VLCD shared pin is set as to the VLCD pin.
Enable the internal voltage adjustment.
The external MCU can detect the voltage of the VLCD pin.
3. When "DE" and "VE" bits are set to {1,0}:
The Segment/VLCD shared pin is set as the Segment pin.
Disable the internal voltage adjustment.
The bias voltage is supplied by the internal V_{DD} power.
The internal voltage follower (OP3) is disabled automatically when DE & VE is set to "10". DA3~DA0 don't care.
4. When "DE" and "VE" bits are set to {1,1}:
The Segment/VLCD shared pin is set as the Segment pin.
Enable the internal voltage adjustment.
5. When the DA0~DA3 bits are set to "0000", the internal voltage follower (OP3) is disabled. When DA0~DA3 bits are set to other values, the internal voltage follower (OP3) is enabled.
6. Power-on status: Enable the internal voltage adjustment and the Segment/VLCD pin is set as the Segment pin.
7. If the programmed command data is not defined, the function will not be affected.

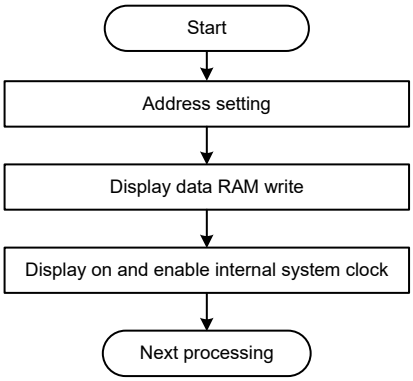
Operation FlowChart

Access procedures are illustrated below by means of flowcharts.

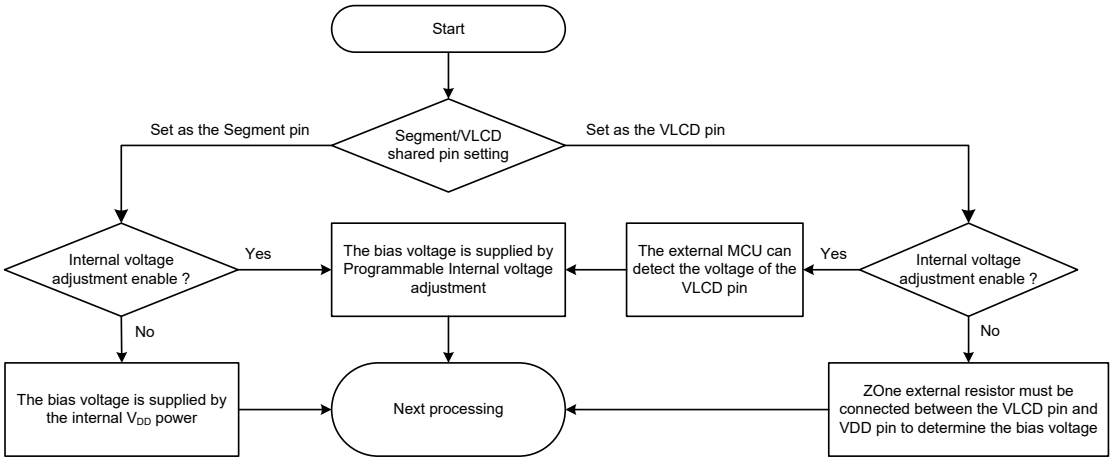
Initialization



Display Data Read/Write (Address Setting)



Segment/VLCD Shared Pin Setting and Internal Voltage Adjustment Setting



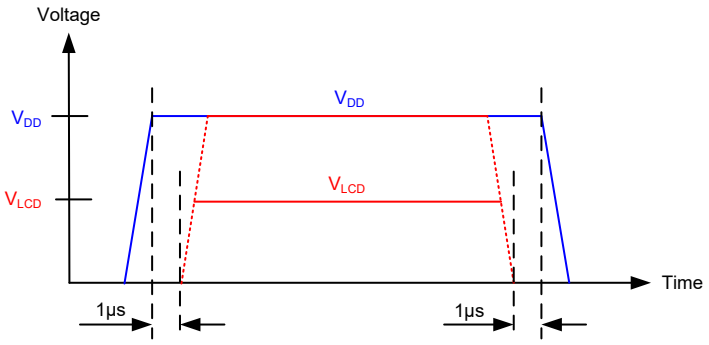
Power Supply Sequence

- If the power is individually supplied on the VLCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

Holtek Power Supply Sequence Requirement:

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD} first and then turn off the logic power supply V_{DD}.

When the V_{LCD} voltage is less than or is equal to V_{DD} voltage application:

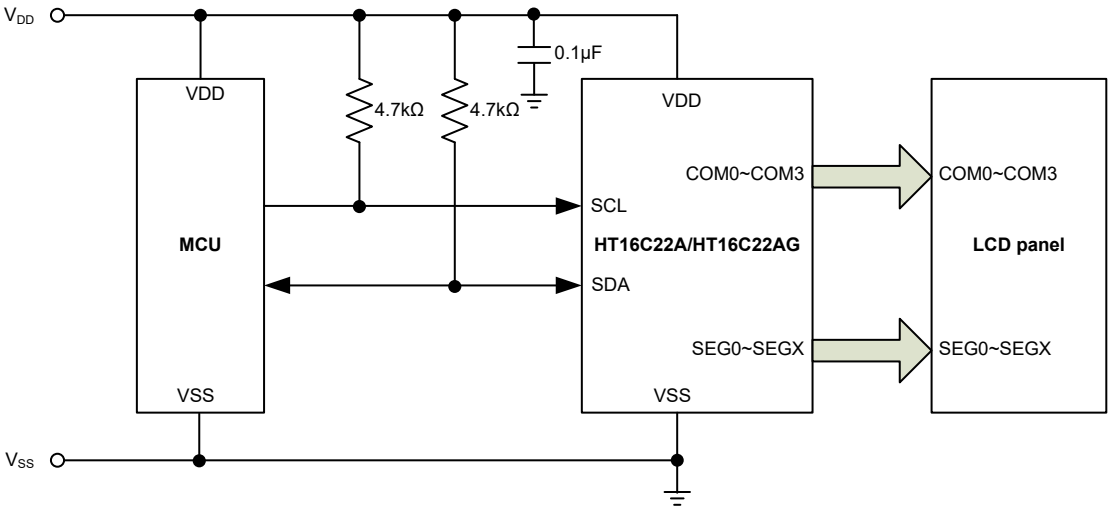


Application Circuits

Set as Segment Pin

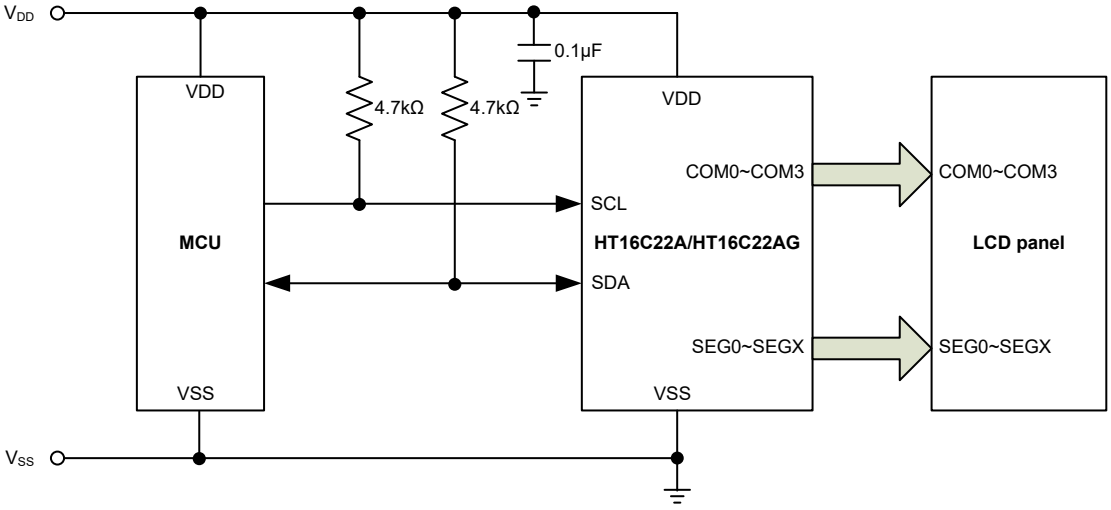
Case 1:

- Disable the internal voltage adjustment.
- The bias voltage is supplied by the internal V_{DD} power.



Case 2:

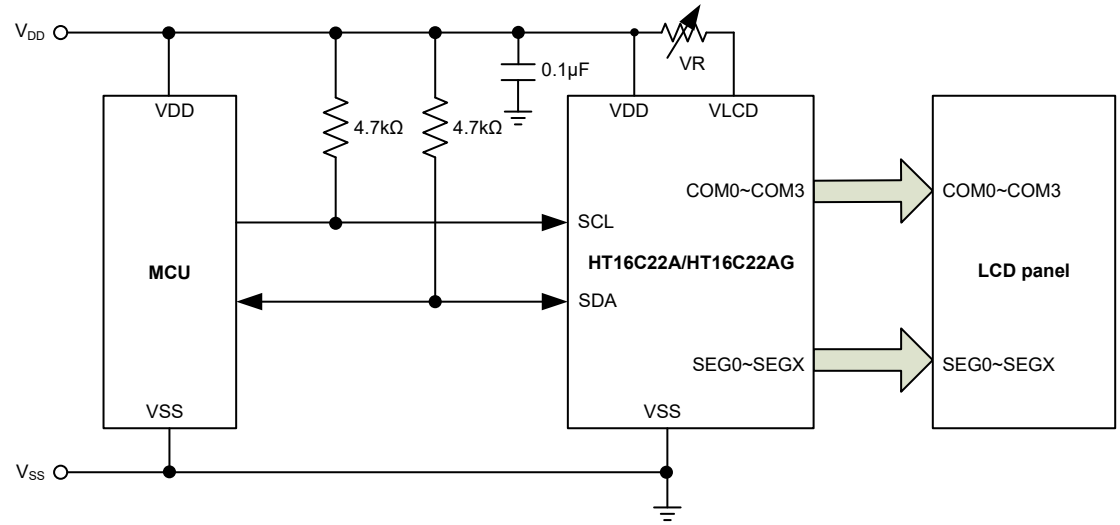
- Enable the internal voltage.
- The internal voltage adjustment for bias voltage.



Set as VLCD Pin

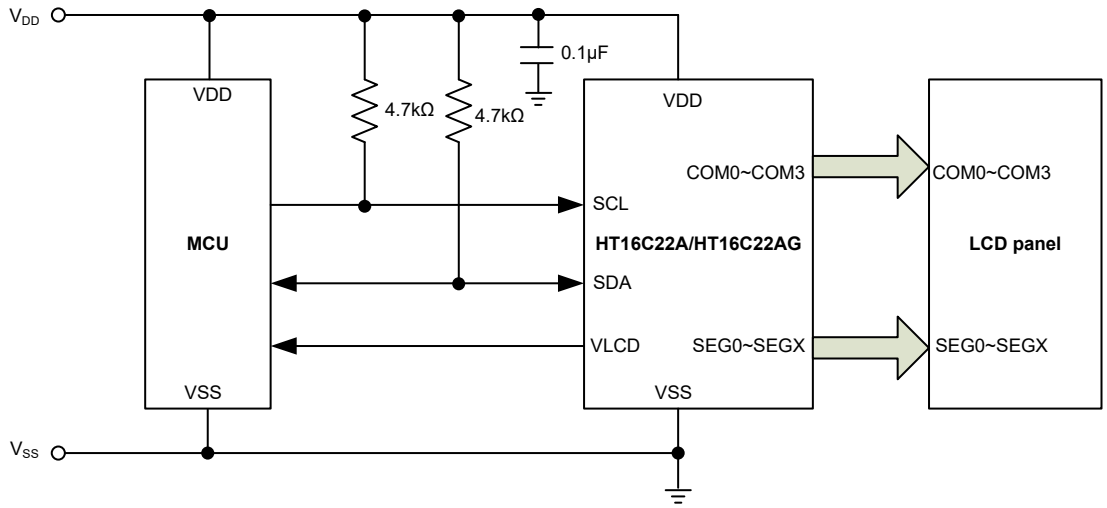
Case 1:

- Disable the internal voltage adjustment.
- One external resister must be connected between the VLCD pin and VDD pin to determine the bias voltage.



Case 2:

- Enable the internal voltage adjustment.
- The external MCU can detect the voltage of VLCD pin.



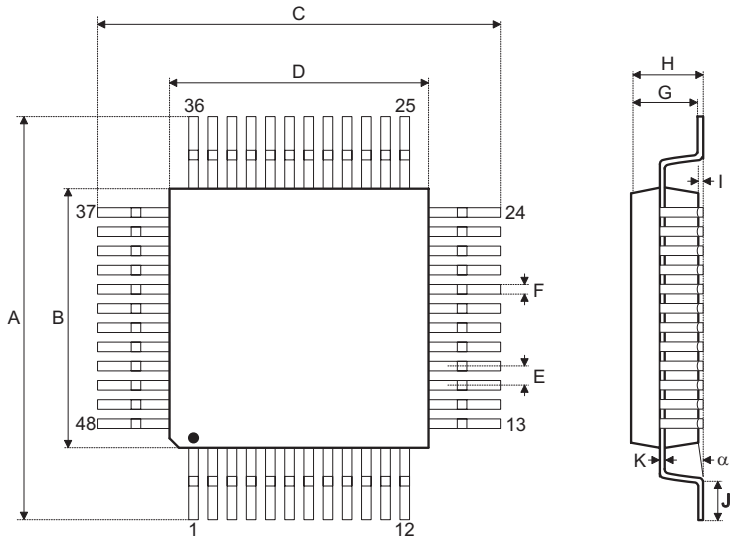
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consul

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

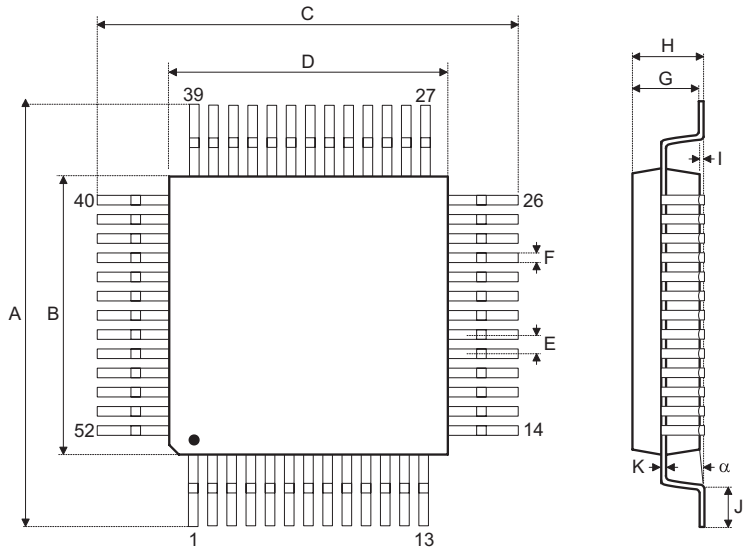
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

52-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.622	0.630	0.638
B	0.547	0.551	0.555
C	0.622	0.630	0.638
D	0.547	0.551	0.555
E	—	0.039 BSC	—
F	0.015	—	0.019
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.008
J	0.018	—	0.030
K	0.005	—	0.007
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	15.80	16.00	16.20
B	13.90	14.00	14.10
C	15.80	16.00	16.20
D	13.90	14.00	14.10
E	—	1.00 BSC	—
F	0.39	—	0.48
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.20
J	0.45	—	0.75
K	0.13	—	0.18
α	0°	—	7°