

# **AC6323A Datasheet**

**Zhuhai Jieli Technology Co.,LTD**

**Version: V1.0**

**Date: 2021.03.06**

**Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.**

## AC6323A Features

### High performance 32-bit RISC CPU

- RISC 32-bit CPU
- DC-96MHz operation
- 73KB data RAM
- 8KB I-cache 2way
- 1KB Rocache 1way
- 64 Vectored interrupts
- 8 Levels interrupt priority

### Flexible I/O

- 17 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level schmitt triggered input
- External wake up/interrupt on all GPIOs

### Peripheral Feature

- One Full Speed USB OTG controller
- Four Multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex advanced UART(DMA)
- Three SPI interface supports host and device mode (DMA)
- One IIC interface supports host and device mode
- RTC,with alarm clock and time base to wake up the chip
- 16-bit PWM generator for motor driving
- Three IQ Encoder
- 8 channels 10-bit ADC
- 1 channel 8 levels Low Power Detector

- Embedded PMU support low power mode
- 2 Crystal Oscillator
- Watchdog
- Power-on reset

### Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth
- V5.0+BR+EDR+BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Support GFSK and  $\pi/4$  DQPSK all packet types
- Provides +8dbm transmitting power
- Receiver with -92dBm sensitivity
- Support  
a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile

### Power Supply

- LDOIN is 4.5V to 5.5V
- VBAT is 1.8V to 4.5V
- VDDIO is 1.8V to 3.4V

### Packages

- QFN20

### Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

# 1. Block Diagram

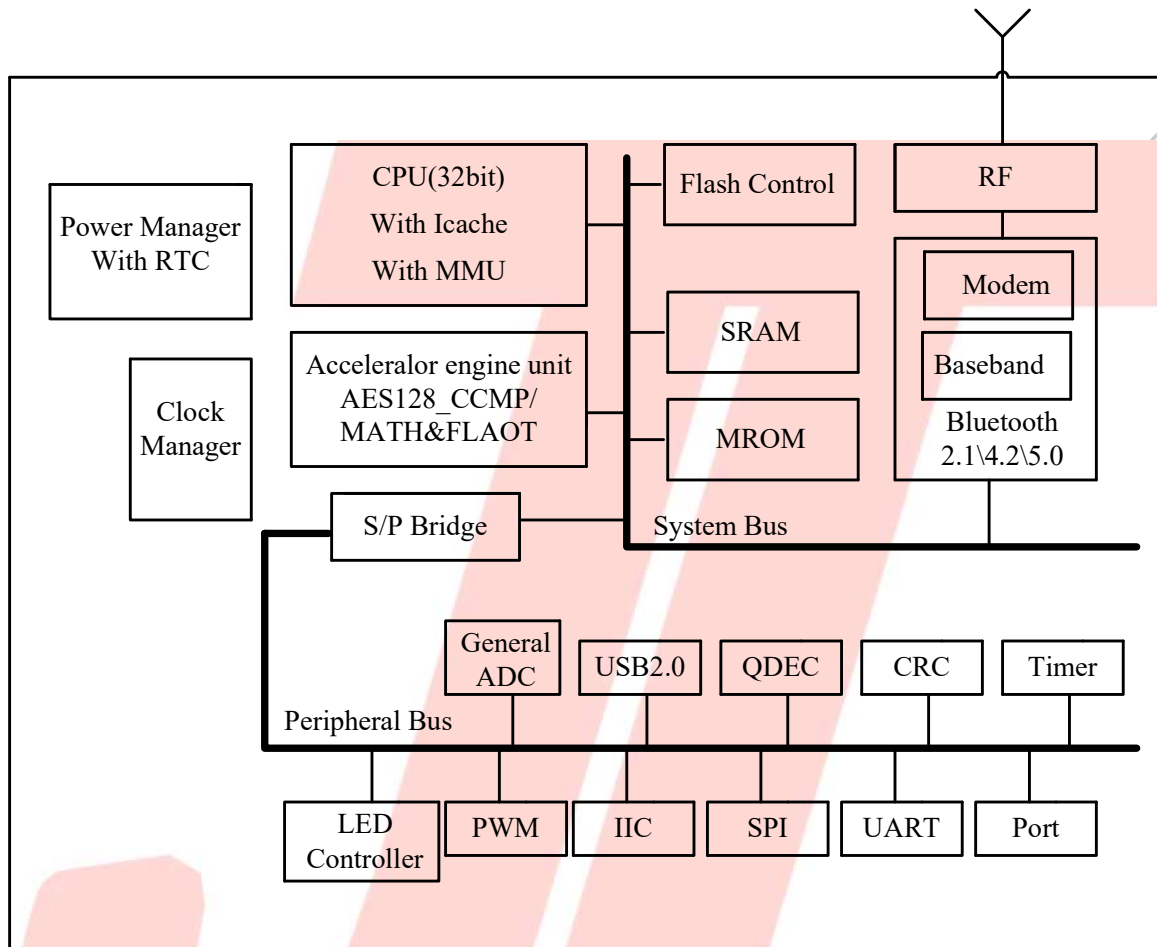


Figure 1-1 AC6323A\_QFN20 Block Diagram

## 2. Pin Definition

### 2.1 Pin Assignment

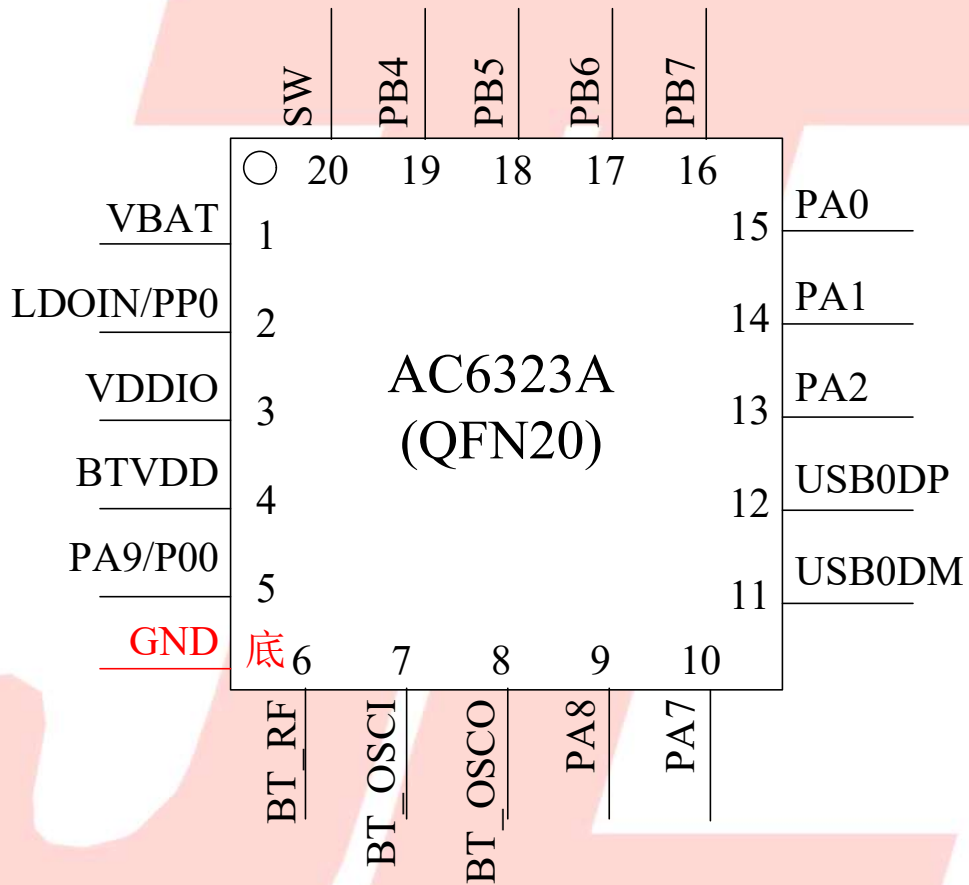


Figure 2-1 AC6323A\_QFN20 Package Diagram

## 2.2 Pin Description

Table 2-1 AC6323A\_QFN20 Pin Description

PIN NO.	Name	I/O Type	Function	Other Function
1	VBAT	P	LDO Power	-
2	LDOIN/PP0	P	Charge Power 5V	PWM3: Timer3 PWM Output; UART0_TXD: Uart0 Data Out(D); UART0_RXD: Uart0 Data In(D);
3	VDDIO	P	IO Power 3.3V	-
4	BTAVDD	P	Core Power 1.3V	-
5	PA9	I/O	GPIO (pull up)	Long Press Reset; ADC8: ADC Channel 8;
	P00	I/O	GPIO (High Voltage)	
6	BT_RF	-	RF Antenna	-
7	BTOSCI	I	BTOSCI	-
8	BTOSCO	O	BTOSCO	-
9	PA8	I/O	GPIO	TMR3: Timer3 Clock In; SPI1_DOA: SPI1 Data Out(A); IIC_SDA_C: IIC SDA(C); ADC4: ADC Channel 4; UART1_RXC: Uart1 Data In(C); PWMCH1L;
10	PA7	I/O	GPIO	TMR1: Timer1 Clock In; SPI1_CLKA: SPI1 Clock(A) ; IIC_SCL_C: IIC SCL(C); ADC3: ADC Channel 3; UART1_TXC: Uart1 Data Out(C); PWMCH1H;
11	USB0DM	I/O	GPIO (pull down)	SPI2_DOB: SPI2 Data Out(B); IIC_SDA_A: IIC SDA(A); ADC11: ADC Channel 11; UART1_RXD: Uart1 Data In(D);

### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

12	USB0DP	I/O	GPIO (pull down)	SPI2_CLKB: SPI2 Clock(B); IIC_SCL_A: IIC SCL(A); ADC10: ADC Channel 10; UART1_TXD: Uart1 Data Out(D);
13	PA2	I/O	GPIO	CAP3: Timer3 Capture; Q-decoder0_1; UART0_RXC: Uart0 Data In(C); UART1_RTS;
14	PA1	I/O	GPIO	PWM0: Timer0 PWM Output; Q-decoder0_0; ADC0: ADC Channel 0; UART0_TXC: Uart0 Data Out(C); UART1_CTS;
15	PA0	I/O	GPIO (High Voltage)	CLKOUT1; UART2_TXB: Uart2 Data Out(B); UART2_RXB: Uart2 Data In(B); PWMCH0H;
16	PB7	I/O	GPIO (High Voltage)	SPI2_DOA: SPI2 Data Out(A); UART2_RXC: Uart2 Data In(C);
17	PB6	I/O	GPIO	SPI2_CLKA: SPI2 Clock(A) ; ADC12: ADC Channel 12; UART2_TXC: Uart2 Data Out(C); TMR3CK;
18	PB5	I/O	GPIO (High Voltage)	SPI2_DIA: SPI2 Data In(A); UART1_RXA: Uart1 Data In(A); PWMCH3L;
19	PB4	I/O	GPIO	TMR2: Timer2 Clock In; Q-decoder2_0; SPI1_DIB: SPI1 Data In(B); ADC9: ADC Channel 9; UAR1_TXA: Uart1 Data Out(A); PWMCH3H;
20	SW	P	DC-DC Switch Pin	-
	Substrate	P	GND	-

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 3. Electrical Characteristics

### 3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T <sub>opt</sub>	Operating temperature	-40	+85	°C
T <sub>stg</sub>	Storage temperature	-65	+150	°C
V <sub>BAT</sub>	Supply Voltage	-0.3	4.5	V
LDO_IN	Charge Input Voltage	-0.3	6	V
V <sub>3.3IO</sub>	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

### 3.2 Recommended Operating Conditions

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>BAT</sub>	Voltage Input	1.8	3.7	4.5	V	—
LDOIN	Voltage Input	4.5	5.0	5.5	V	—
V <sub>DIO</sub>	Voltage output	1.8	3.0	3.4	V	V <sub>BAT</sub> = 4.2V, 60mA loading
BTA <sub>VDD</sub>	Voltage output	1	1.3	1.4	V	DC-DC mode: 40mA loading
IL <sub>3.3</sub>	Loading current	—	—	60	mA	V <sub>BAT</sub> = 4.2V

### 3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Charge Input Voltage	4.5	5	5.5	V	—
V <sub>Charge</sub>	Charge Voltage	4.15	4.2	4.25	V	—
I <sub>Charge</sub>	Charge Current	20		200	mA	Charge current at fast charge mode
I <sub>Trinkl</sub>	Trickle Charge Current	20	45	70	mA	V <sub>BAT</sub> < V <sub>Trinkl</sub>

#### Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

### 3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>IL</sub>	Low-Level Input Voltage	-0.3	–	0.3* VDDIO	V	VDDIO = 3.3V
V <sub>IH</sub>	High-Level Input Voltage	0.7* VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V <sub>OL</sub>	Low-Level Output Voltage	–	–	0.33	V	VDDIO = 3.3V
V <sub>OH</sub>	High-Level Output Voltage	2.7	–	–	V	VDDIO = 3.3V

### 3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive Strength	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1-PA9, PB4,PB6,	drive_select[11] 24mA drive_select[10] 24mA (with 120ohm res) drive_select[01] 8mA drive_select[00] 8mA (with 120ohm res)	10K	10K	1. PA9&PB2 default pull up 2. USB0DM&USB0DP default pull down 3. Internal pull-up/pull-down resistance   accuracy ±20% 4.PA0,PB5,PB7 can pull-up resistance to 5V
PA0,PB5, PB7	8mA	10K	10K	
USB0DP	4mA	1.5K	15K	
USB0DM	4mA	180K	15K	

### 3.6 BT Characteristics

#### 3.6.1 Transmitter

Basic Data Rate

Table 3-6

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		4	6	dBm	25°C, Power Supply VBAT=5V
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	



	-2MHz		-38		dBm
	+3MHz		-44		dBm
	-3MHz		-35		dBm

**Enhanced Data Rate** **Table 3-7**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1		dB	
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS		7		%	25°C, Power Supply
	DEVM 99%		12		%	
	DEVM Peak		17		%	
Adjacent Channel	+2MHz		-40		dBm	VBAT=5V 2441MHz
	-2MHz		-38		dBm	
Transmit Power	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

**3.6.2 Receiver****Basic Data Rate** **Table 3-8**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	
Co-channel Interference Rejection			-9		dB	
Adjacent Channel	+1MHz		+5		dB	25°C, Power Supply
	-1MHz		+2		dB	
	+2MHz		+37		dB	
Interference Rejection	-2MHz		+36		dB	VBAT=5V 2441MHz
	+3MHz		+40		dB	
	-3MHz		+35		dB	

**Enhanced Data Rate** **Table 3-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	
Co-channel Interference Rejection			-9		dB	
Adjacent Channel	+1MHz		+5		dB	25°C, Power Supply
	-1MHz		+2		dB	
	+2MHz		+37		dB	
Interference Rejection	-2MHz		+36		dB	VBAT=5V 2441MHz
	+3MHz		+40		dB	
	-3MHz		+35		dB	

**Confidential**

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

## 4. Package Information

### 4.1 QFN20

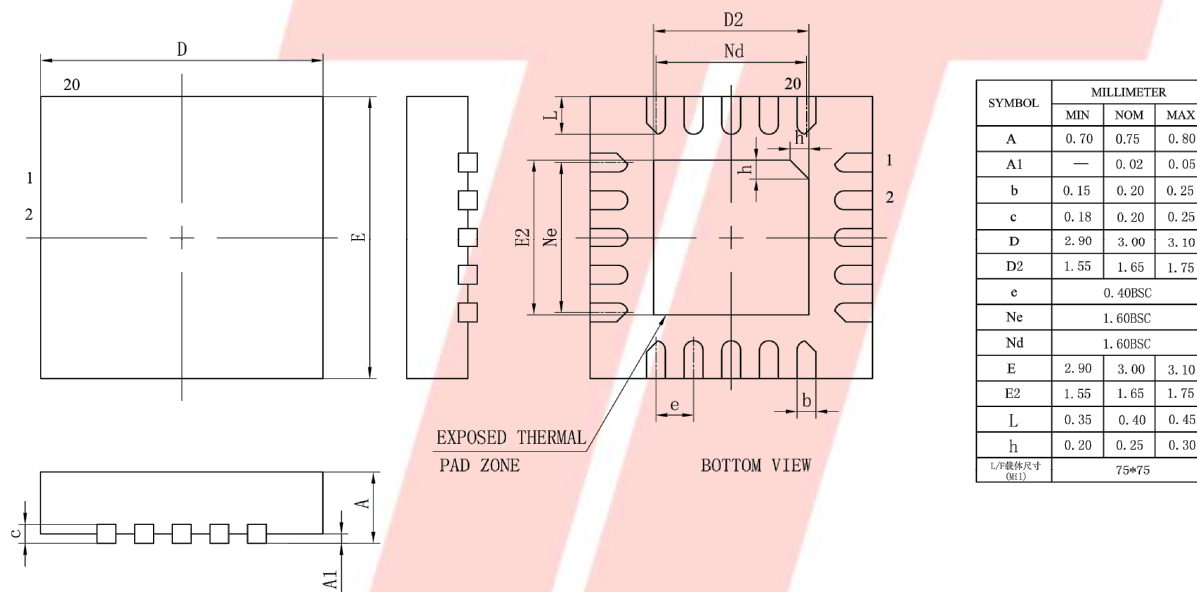
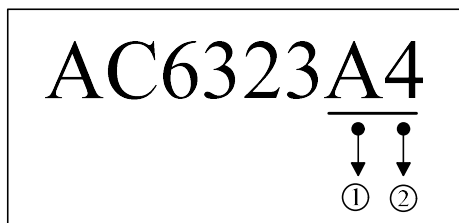


Figure 4-1 AC6323A\_QFN20 Package

## 5. Package Type Specification



① Represents different packages

② Represents different memory sizes

2: 2Mbit Flash

4: 4Mbit Flash

## 6. Revision History

Date	Revision	Description
2021.03.06	V1.0	Initial Release