

AC6954C Datasheet

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Version: V1.1

Date: 2020.07.20

AC6954C Features

CPU

- 32-bit DSP supports hardware Float Point Unit (FPU)
- Up to 240MHz programmable processor
- 64 Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codecs supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC, AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 30-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC, SNR \geq 92dB
- Three channels 16-bit ADC, SNR \geq 90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- three channels Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.1+BR+EDR+BLE specification

- Meet class1 class2 and class3 transmitting power requirement
- Support GFSK and $\pi/4$ DQPSK all packet types
- Provides +6dbm transmitting power
- receiver with -90dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile

Peripherals

- One full speed USB 2.0 OTG controller
 - Two PCM/IIS for external digital Audio code, supports host and device mode
 - Four multi-function 16-bit timers, support capture and PWM mode
 - Three 16-bit PWM generator for motor driving
 - Three full-duplex basic UART, UART0 and UART1 supports DMA mode
 - Three SPI interface supports host and device mode
 - Two SD Card Host controller
 - One hardware IIC interface supports host and device mode
 - Four SPDIF receiving interface without analog amplify
 - Supports HDMI ARC (Audio Return Channel) receiving
 - Segment LCD panels
 - Digital matrix LED panels
 - Built-in Cap Sense Key controller
 - 10-bit ADC for analog sampling
 - External wake up/interrupt on all GPIOs
- ## PMU
- Low voltage LDO for internal digital and analog circuit supply
 - 3uA current consumption in the soft-off mode
 - Built-in LDO for the core, I/O, Bluetooth and flash

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- VBAT is 2.2V to 5.5V
- VDDIO is 2.2V to 3.6V
- RTCVDD33 is 2.2V to 3.6V

Packages

- LQFP52(6mm*6mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth Stereo speaker
- Bluetooth soundbar
- Bluetooth car speaker
- Bluetooth TWS speaker
- Bluetooth alarm clock speaker
- Bluetooth Rod speaker
- Bluetooth Watch

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1、 Pin Definition

1.1 Pin Assignment

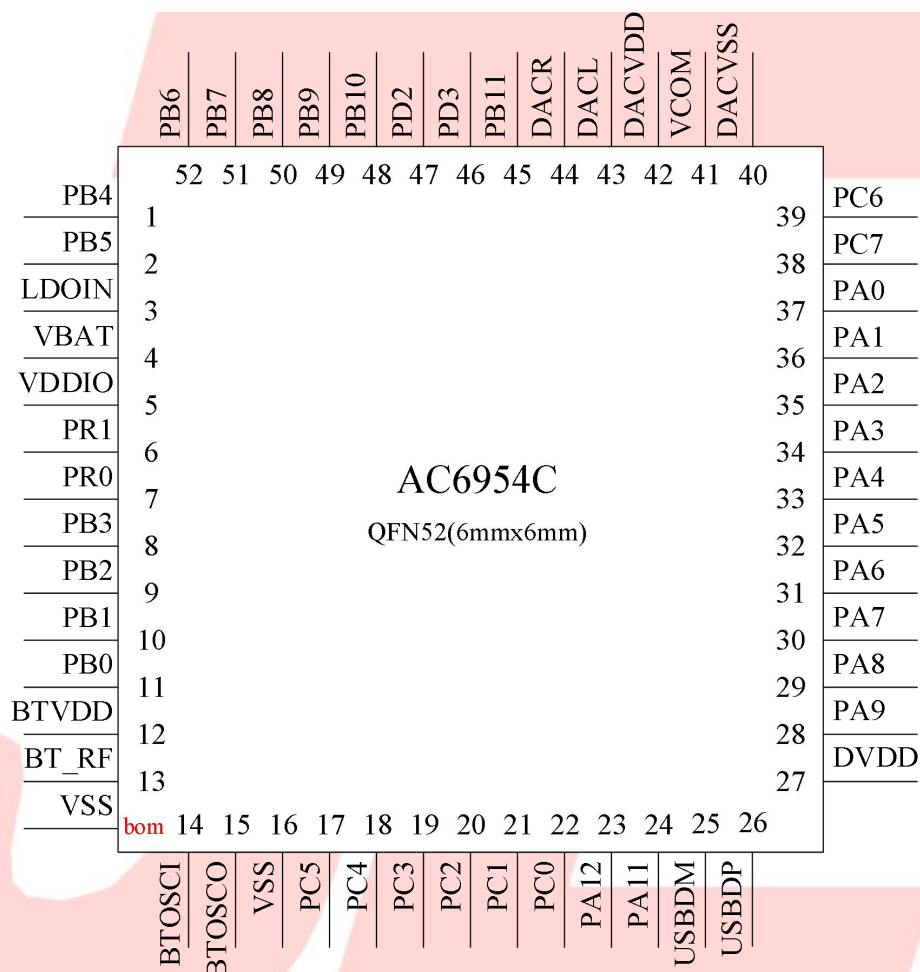


Figure 1-1 AC6954C Package Diagram

1.2 Pin Description

Table 1-1 AC6954C Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	PB4	I/O	24/8	GPIO	SD1DAT0B: SD1 Data0(B); SD0DAT3B: SD0 Data3(B); IIC_SCL_C: IIC SCL(C); ADC7: ADC Input Channel 7; UART0TXB: Uart0 Data Out(B); LVD: Low Voltage Detect Input; PWMCH2H: Motor PWM Channel2 (H);
2	PB5	I/O	8	GPIO (High Voltage Resistance)	SD1CMDB: SD1 Command(B); SD0DAT2B: SD1 Data2(B); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture; UART0TXC: Uart0 Data Out(C); UART0RXC: Uart0 Data In(C);
3	LDOIN	P	/		Battery Charge Input
4	VBAT	P	/		Power Supply
5	VDDIO	P	/		IO Power 3.3v
6	PR1	I/O	8	RTCIO1	OSCO_32K
7	PR0	I/O	8	RTCIO0	OSCI_32K
8	PB3	I/O	24/8	GPIO	PWM2: Timer2 PWM Output; ADC6: ADC Input Channel 6;
9	PB2	I/O	8	GPIO (High Voltage Resistance)	SPI1DIA: SPI1 Data In(A); PWMCH1L: Motor PWM Channel1 (L);
10	PB1	I/O	24/8	GPIO (pull up)	Long Press Reset; SPI1DOA: SPI1 Data Out(A); ADC5: ADC Input Channel 5; TMR2: Timer2 Clock Input; UART1RXA: Uart1 Data In(A); SPDIF_IN_D: Sony/Philips Digital Interface Input(D)

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11	PB0	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKA: SPI1 Clock(A); ALNK1_MCLK: ALNK1 Master Clock; SPDIF_IN_C: Sony/Philips Digital Interface Input(C) UART1TXA: Uart1 Data Out(A); PWMCH1H: Motor PWM Channel1(H);
12	BTVDD	P	/		BT Power
13	BT_RF	/	/		BT Antenna
14	BTOSCI	I	/		BT OSC In
15	BTOSCO	O	/		BT OSC Out
16	VSS	P	/		Ground
17	PC5	I/O	24/8	GPIO	SD1CLKA: SD1 Clock(A); SPI1DOB: SPI1 Data Out(B); UART2RXD: Uart2 Data In(D); IIC_SDA_B: IIC SDA(B); ALNK1_DAT3: Audio Link Data3; ADC13: ADC Input Channel 13; PAPD7: PAP Data 7; Touch15: Touch Input Channel 15; PWMCH5L: Motor PWM Channel5(L);
18	PC4	I/O	24/8	GPIO	SD1CMDA: SD1 Command(A); SPI1CLKB: SPI1 Clock(B); UART2TXD: Uart2 Data Out(D); IIC_SCL_B: IIC SCL(B); ALNK1_DAT2: Audio Link Data2; ADC10: ADC Input Channel 10; Touch14: Touch Input Channel 14; PWMCH5H: Motor PWM Channel5(H);
19	PC3	I/O	24/8	GPIO	SD1DAT0A: SD1 Data0(A); SPI1DIB: SPI1 Data In(B); ALNK1_DAT1: Audio Link Data1; Touch13: Touch Input Channel 13;
20	PC2	I/O	24/8	GPIO	SD1DAT1A: SD1 Data1(A); ALNK1_DAT0: Audio Link Data0; Touch12: Touch Input Channel 12; FPIN5: Motor Auto-Stop Protective Pin5;
21	PC1	I/O	24/8	GPIO	SD1DAT2A: SD1 Data2(A); ALNK1_LRCK: Audio Link Word Select; Touch11: Touch Input Channel 11; UART1RXB: Uart1 Data In(B); FPIN4: Motor Auto-Stop Protective Pin4;

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22	PC0	I/O	24/8	GPIO	SD1DAT3A: SD1 Data3(A); ALNK1_SCLK: Audio Link Serial Clock; Touch10: Touch Input Channel 10; UART1TXB: Uart1 Data Out(B); FPIN3: Motor Auto-Stop Protective Pin3;
23	PA12	I/O	24/8	GPIO	PWM1: Timer1 PWM Output; ADC4: ADC Input Channel 4; UART0RXD: Uart0 Data In(D);
24	PA11	I/O	24/8	GPIO	UART0TXD: Uart0 Data Out(D);
25	USBDM	I/O	4	USB Negative Data (pull down)	UART1RXD: Uart1 Data In(D); SPI2DOB: SPI2 Data Out(B); IIC_SDA_A: IIC SDA(A);
26	USBDP	I/O	4	USB Positive Data (pull down)	UART1TXD: Uart1 Data Out(D); SPI2CLKB: SPI2 Clock(B); IIC_SCL_A: IIC SCL(A); ADC12: ADC Input Channel 12;
27	DVDD	P			System Power
28	PA9	I/O	24/8	GPIO	SPDIF_IN_A: Sony/Philips Digital Interface Input(A) Touch8: Touch Input Channel 8; UART2TXB: Uart2 Data Out(B); PWMCH4H: Motor PWM Channel4(H);
29	PA8	I/O	24/8	GPIO	SPI0DOC: SPI0 Data0 Out(C); ALNK0_MCLKA: ALNK Master Clock(A); BT_Freq; FPIN2: Motor Auto-Stop Protective Pin2;
30	PA7	I/O	24/8	GPIO	SPI0D2C: SPI0 Data2(C); ALNK0_DAT3A: Audio Link Data3(A); BT_priority; TMR0: Timer0 Clock Input; Touch7: Touch Input Channel 7;
31	PA6	I/O	24/8	GPIO	SPI0DIC: SPI0 Data1 In(C); ALNK0_DAT2A: Audio Link Data2(A); ADC2: ADC Input Channel 2; Wlan_Active; IIC_SDA_D: IIC SDA(D); Touch6: Touch Input Channel 6; UART0RXA: Uart0 Data In(A);

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32	PA5	I/O	24/8	GPIO	ALNK0_DAT1A: Audio Link Data1(A); ADC1: ADC Input Channel 1; BT_Active; IIC_SCL_D: IIC SCL(D); Touch5: Touch Input Channel 5; PWM0: Timer0 PWM Output; UART0TXA: Uart0 Data Out(A);
33	PA4	I/O	24/8	GPIO	SPI0CSC: SPI0 Chip Selection(C); ALNK0_DAT0A: Audio Link Data0(A); Touch4: Touch Input Channel 4;
34	PA3	I/O	24/8	GPIO	SPI0CLKC: SPI0 Clock(C); PLNK_DAT1: PLNK Data1; ALNK0_LRCKA: Audio Link Word Select(A); Touch3: Touch Input Channel 3; UART2RXA: Uart2 Data In(A);
35	PA2	I/O	24/8	GPIO	SPI0D3C: SPI0 Data3(C); PLNK_SCLK: PLNK Serial Clock; ALNK0_SCLKA: Audio Link Serial Clock(A); Touch2: Touch Input Channel 2; UART2TXA: Uart2 Data Out(A); CAP3: Timer3 Capture;
36	PA1	I/O	24/8	GPIO	AMUX0R: Analog Channel0 Right; Touch1: Touch Input Channel 1; ADC0: ADC Input Channel 0; UART1RXC: Uart1 Data In(C); PWMCH0L: Motor PWM Channel0(L);
37	PA0	I/O	24/8	GPIO	AMUX0L: Analog Channel0 Left; Touch0: Touch Input Channel 0; CLKOUT0; UART1TXC: Uart1 Data Out(C); PWMCH0H: Motor PWM Channel0(H);
38	PC7	I/O	/	GPIO	MIC_BIAS: Microphone Bias Output
39	MIC	I	/		MIC: MIC Input Channel;
40	DACVSS	P	/		DAC Ground
41	VCOM	P	/		DAC Reference
42	DACVDD	P	/		DAC Power
43	DACL	O	/		DAC Left Channel
44	DACR	O	/		DAC Right Channel
45	PB11	I/O	24/8	GPIO	SDPG: SD CARD Power Gate;
46	PD3	I/O	24/8	GPIO	-
47	PD2	I/O	24/8	GPIO	-

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48	PB10	I/O	24/8	GPIO	AMUX2R: Analog Channel2 Right; SD0CMB: SD0 Command(B); SPI2DOA: SPI2 Data Out(A); SD1DAT3B: SD1 Data3(B); ADC9: ADC Input Channel 9; UART2RXC: Uart2 Data In(C); PWMCH3L: Motor PWM Channel3(L);
49	PB9	I/O	24/8	GPIO	AMUX2L: Analog Channel2 Left; SD0CLKB: SD0 Clock(B); SPI2CLKA: SPI2 Clk(A); SD1DAT2B: SD1 Data2(B); CAP0: Timer0 Capture; UART2TXC: Uart2 Data Out(C); PWMCH3H: Motor PWM Channel3(H);
50	PB8	I/O	24/8	GPIO	AMUX1R: Analog Channel1 Right; SD0DAT0B: SD0 Data0(B); SPI2_DIA: SPI2 Data In(A); SD1DAT1B: SD1 Data1(B); ADC8: ADC Input Channel 8; CLKOUT1: Clk Out1;
51	PB7	I/O	24/8	GPIO	AMUX1L: Analog Channel1 Left;
52	PB6	I/O	24/8	GPIO	SD1CLKB: SD1 Clock(B); SD0DAT1B: SD0 Data1(B); IIC_SDA_C: IIC SDA(C); TMR3: Timer3 Clock Input; UART0RXB: Uart0 Data In(B); PWMCH2L: Motor PWM Channel2 (L);

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2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	2.2	5.5	V
LDO_IN	Charger Voltage	4.5	5.5	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	—
LDO_IN	Charger Voltage	4.5	5.0	5.5	V	—
V _{DDIO}	Voltage output	—	3.3	—	V	VBAT = 5V, 100mA loading
V _{BTVD}	Voltage output	—	1.3	—	V	VBAT=5V, 100mA loading
I _{L3.3}	Loading current	—	—	150	mA	VBAT = 5V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	—	0.3* V _{DDIO}	V	V _{DDIO} = 3.3V
V _{IH}	High-Level Input Voltage	0.7* V _{DDIO}	—	V _{DDIO} +0.3	V	V _{DDIO} = 3.3V
IO output characteristics						
V _{OL}	Low-Level Output Voltage	—	—	0.33	V	V _{DDIO} = 3.3V
V _{OH}	High-Level Output Voltage	2.7	—	—	V	V _{DDIO} = 3.3V

2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA12 PB1 PB3, PB4 PB6~PB10 PC0~PC5 PD2, PD3	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、PB0, PB2, PB5 are high voltage resistance to 5V 4、internal pull-up/pull-down resistance accuracy $\pm 20\%$ 5、PRx supply by RTCVDD
(driving low) PB11, PC7	8mA	24mA	10K	10K	
(driving high)	8mA	64mA			
PB0, PB2, PB5	8mA	–	10K	10K	
PR0-PR1	8mA	–	10K	10K	
USBDP	4mA	–	1.5K	15K	
USBDM	4mA	–	180K	15K	

2.5 DAC Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	–	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	–	-75	–	dB	
S/N	–	92	–	dB	
Crosstalk	–	-80	–	dB	
Output Swing	–	1	–	Vrms	
Dynamic Range	–	90	–	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	11	–	–	mW	32ohm loading

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2.6 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	–	80	–	dB	1KHz/-60dB
S/N	–	90	91	dB	1KHz/-60dB
THD+N	–	-70	–	dB	
Crosstalk	–	-80	–	dB	

2.7 BT Characteristics

2.7.1 Transmitter

Basic Data Rate

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		4	6	dBm	25°C, Power Supply VBAT=5V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Enhanced Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
Relative Power		-1		dB	25°C, Power Supply VBAT=5V 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS	6		%	
	DEVM 99%	10		%	
	DEVM Peak	15		%	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

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2.7.2 Receiver

Basic Data Rate

Table 2-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
Interference Rejection	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate

Table 2-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=5V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
Interference Rejection	+2MHz		+37		dB	
	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

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3、 Package Information

3.1 QFN52(6mm*6mm)

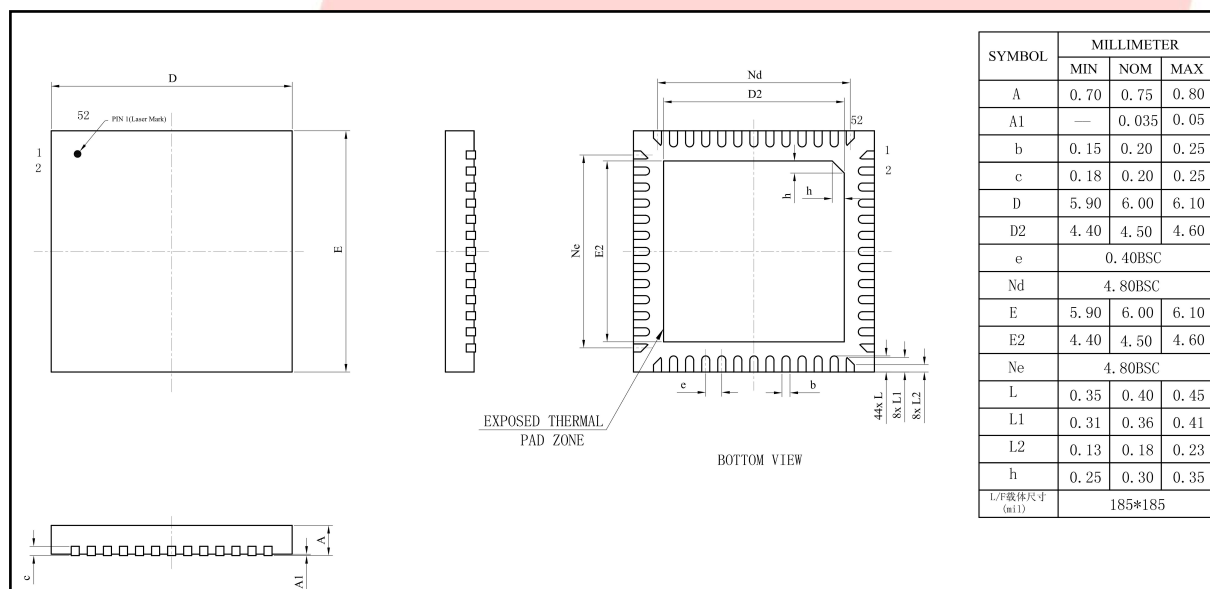


Figure 3-1. AC6954C Package

3、 Revision History

Date	Revision	Description
2020.07.20	V1.0	Initial Release