CMS80F751x Datasheet

Enhanced 1T 8051 microcontroller with flash memory

Rev. 1.06

1. Product Features

1.1 Features

- **Compatible with MCS-51 1T Instruction System**
  - System clock frequency supports up to 48MHz
  - Machine cycle maximum $1T_{SYS}$ @ $F_{SYS} \leq 24MHz$
  - Machine cycle maximum $2T_{SYS}$ @ $F_{SYS} = 48MHz$
- **Memory**
  - Program FLASH：32K×8Bit
  - Data FLASH：1K×8Bit
  - IRAM：256×8Bit
  - XRAM：2K×8Bit
  - Support BOOT function area,1K/2K/4K optional
  - Program FLASH supports partition protection
- **4 Oscillation Modes**
  - HSI-Internal high-speed oscillator: 48MHz
  - HSE-External high-speed oscillator: 8MHz/16MHz
  - LSE-External low-speed oscillator: 32.768KHz
  - LSI-Internal low-speed oscillator: 125KHz
- **GPIO**
  - Up to 30 GPIOs
  - Support pull-up/down resistor function
  - Support edge (rising edge/falling edge/both edge) interrupt
  - Support wake-up function
- **Interrupts**
  - Support all external port interrupts
  - Up to 7 timer interrupts
  - Other peripheral interrupts
- **Timers**
  - WDT（watchdog timer）
  - Timer0/1，Timer2，Timer3/4
  - LSE Timer（Support wake up）
  - WUT (wake-up timer）
  - BRT（baud rate clock generation timer）
- **Cyclic Redundancy Check Unit**
  - CRC16（CRC16-CCITT）
- **Multiplication and Division Operation Unit (MDU)**
  - Support 32bit/16bit, 16bit/16bit, 16bit×16bit
- **Buzzer Driver**
  - 50% duty cycle, frequency can be set freely
- **Enhanced PWM**
  - 6 channels enhanced PWM
  - 6 independent cycle counters
  - Support independent /complementary/ synchronous/ group mode
  - Support edge alignment/center alignment
  - Support complementary mode dead zone delay function
- **Communication Module**
  - 1xSPI(communication rate up to 6Mb/s)
  - 1xI2C (communication rate up to 400Kb/s)
  - 2xUART (baud rate up to 1Mb/s)
  - UART1 can be mapped to any GPIO
- **Operating Voltage Range**
  - 2.1V～5.5V
- **Operating Temperature Range**
  - -40℃～105℃
- **Low-voltage Reset Function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low-voltage Detection Function (LVD)**
  - 2.0V ~ 4.6V, 16 levels optional
- **Built-in Temperature Sensor（TS）**
- **High precision 12-bit ADC**
  - Up to 30 AD external channels
  - Optional reference voltage (1.2V/2.0V/2.4V/3.0V/VDD)
  - Can detect internal 1.2V reference voltage
  - Support hardware trigger start conversion function
  - Support a set of result digital comparison function
- **Hardware LCD Driver**
  - Optional duty cycle: 1/4, 1/5, 1/6, 1/8
  - Optional three clock sources: LSI/LSE/system clock
  - Traditional resistive LCD, optional BIAS: 1/2, 1/3, 1/4
  - Support work in sleep mode
  - Support fast charging mode
  - Support energy-saving mode, the total resistance of voltage divider can be 60K/225K/900K
  - Support up to 4COM x 20SEG, 5COM x 19SEG, 6COM x 18SEG, 8COM x 16SEG
- **Hardware LED Driver**
  - Optional duty cycle: 1/4, 1/5, 1/6, 1/8
  - Support two modes: common cathode/common anode
  - Optional three clock sources: LSI/LSE/system clock
  - Optional COM, SEG current
  - Support up to 4COM x 20SEG、5COM x 19SEG, 6COM x 18SEG、8COM x 16SEG
- **High Sensitivity Touch**
- **Two analog comparators（ACMP0/1）**
  - 4 options for the positive terminal, internal 1.2V/VDD divider for the negative terminal
  - Comparator supports unilateral/bilateral hysteresis
  - The internal 1.2V/VDD divider of the negative terminal can be connected to the internal ADC channel l
- **Two Amplifiers（OP0/1）**
  - Three terminals of each operational amplifier are multiplexed with GPIO port
  - The positive terminal supports internal 1.2V input
  - Support two modes of operational amplifier /comparator
  - The output of the operational amplifier can be connected to the input of the internal analog comparator
- **Low Power Mode**
  - Idle mode（IDLE）
  - Sleep mode (STOP)
- **Support 96-bit Unique ID Number (UID)**
  - Each chip has an independent ID number
- **Support Two-wire Serial Programming and Debugging**

1.2 Product Comparison

Product / Peripherals		CMS80F7518	CMS80F7519
Maximum clock frequency		48MHz	
Memory size	APROM	32/31/30/28 KB (1)	
	BOOT	0/1/2/4 KB (1)	
	Data FLASH	1 KB	
	RAM	256 B	
	XRAM	2 KB	
Timer	WDT	1	
	Timer0/1	2 (16bit)	
	Timer2	1 (16bit)	
	Timer3/4	2 (16bit)	
	LSE_Timer	1 (16bit)	
	WUT	1 (12bit)	
	BRT	1 (16bit)	
Enhanced digital peripherals	CRC	CRC16-CCITT	
	MDU	32bit/16bit、16bit/16bit、16bit*16bit	
	BUZZER	1	
	PWM	6(16bit)	
Display interface	LCD	4COM x 16SEG、5COM x 15SEG 6COM x 14SEG、8COM x 12SEG	4COM x 20SEG、5COM x 19SEG 6COM x 18SEG、8COM x 16SEG
	LED	4COM x 16SEG、5COM x 15SEG 6COM x 14SEG、8COM x 12SEG	4COM x 20SEG、5COM x 19SEG 6COM x 18SEG、8COM x 16SEG
Communication	SPI	1	
	I2C	1	
	UART	2	
Analog	12bit-ADC (Number of external channels)	26	30
	TOUCH	26	30
	ACMP	2	
	OP	2	
GPIOs		26	30
LVR		1.8V/2.0V/2.5V/3.5V	
LVD		2.0V ~ 4.6V, 16 levels optional	
Operating voltage		2.1~5.5 V	
Operating temperature		-40~105 ℃	
Package		SOP28	LQFP32

Note: (1) Set the size of APROM and BOOT space through the system configuration register. The maximum total space of APROM and BOOT is 32K.

2. System Overview

2.1 System Introduction

CMS80F751x series is an 8051 core, a 1T instruction system compatible with MCS-51, and a general IO type 8-bit chip. The operating frequency can reach up to 48MHz. The MCU has the following characteristics:

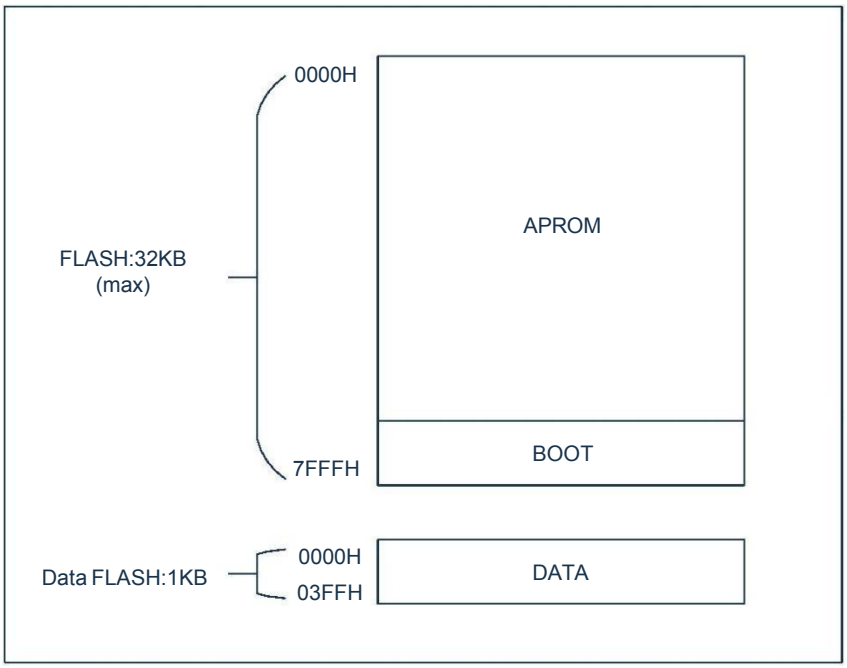
- With a maximum of 32KB program area, 256B RAM space, 2KB XRAM, 1KB Data FLASH area.
- With four oscillation modes.
- It supports 3 working modes: normal, idle , and sleep, which can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage detection LVD, watchdog overflow reset, window watchdog reset and other protection settings can effectively improve the reliability of system operation.
- With multiple interrupt sources such as external interrupts, timer interrupts and other peripheral interrupts, it can respond to external events in a timely manner and improve the utilization of the MCU.
- 9 timers, which can realize functions such as timing, counting, input capture, output comparison, timing wake-up, and baud rate generator.
- With hardware multiplication and division unit MDU, cyclic redundancy check unit CRC.
- LED driver module supports up to 8COM and 20SEG.
- LCD driver module supports up to 8COM and 20SEG.
- 6-channel 16-bit PWM, supports independent, complementary, and synchronous three-mode output, and has hardware brake function, dead zone control function, mask output and other functions.
- With 1 I2C, 1 SPI, and 2 UART communication modules, it can realize data transmission between the system and other devices.
- With high-precision 12-bit ADC and selectable internal reference voltage, up to 2 amplifiers, up to 2 comparators, up to 30 high sensitivity touch channels, built-in temperature sensor (TS），and more abundant analog functions.

2.2 Memory Structure

2.2.1 Program Memory FLASH

This series has a maximum of 32KB of FLASH storage space, APROM area and BOOT area share the entire FLASH space.

The block diagram of the FLASH space allocation structure is as follows:



CMS80F751x can configure the size of BOOT, the configuration method is as follows:

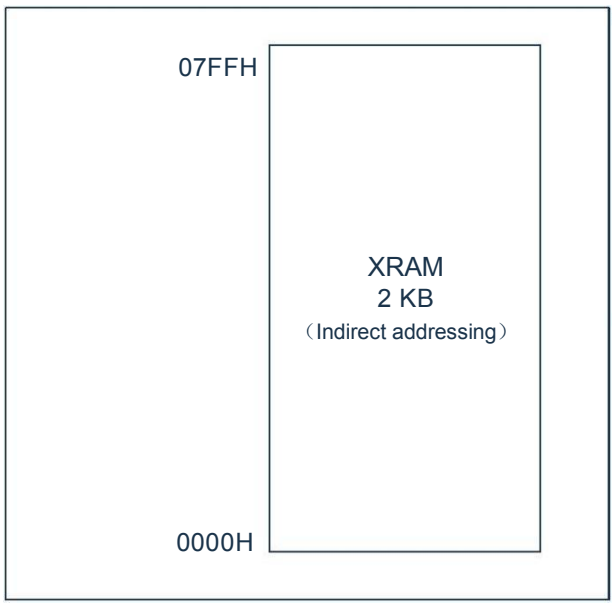
64K (Program storage area)				
Address Space Allocation Method	APROM		BOOT	
Method 0	32K	0000H-7FFFH	--	--
Method 1	31K	0000H-7BFFH	1K	7C00H-7FFFH
Method 2	30K	0000H-77FFH	2K	7800H-7FFFH
Method 3	28K	0000H-6FFFH	4K	7000H-7FFFH

2.2.2 Internal Data Memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The structure diagram of RAM space allocation is shown in the figure below:

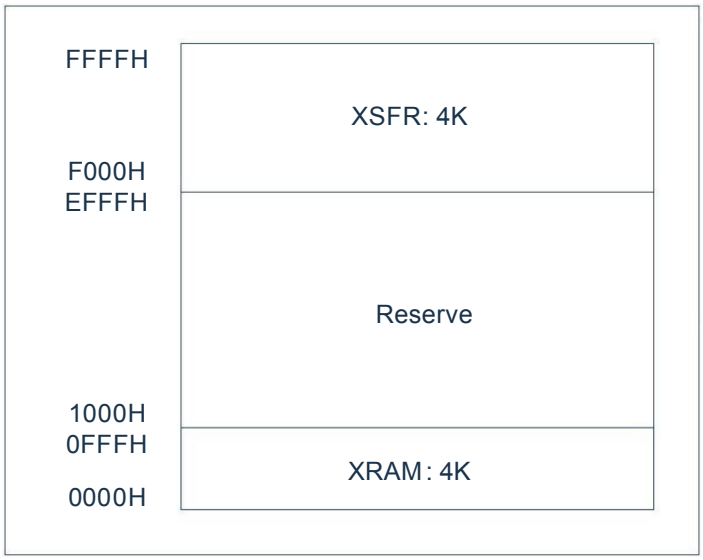
2.2.3 External Data Memory XRAM

There is a maximum 2KB XRAM area inside the chip, which is not related to RAM/FLASH. The structure diagram of XRAM space allocation is shown in the figure below.



2.2.4 Special Function Register XSFR

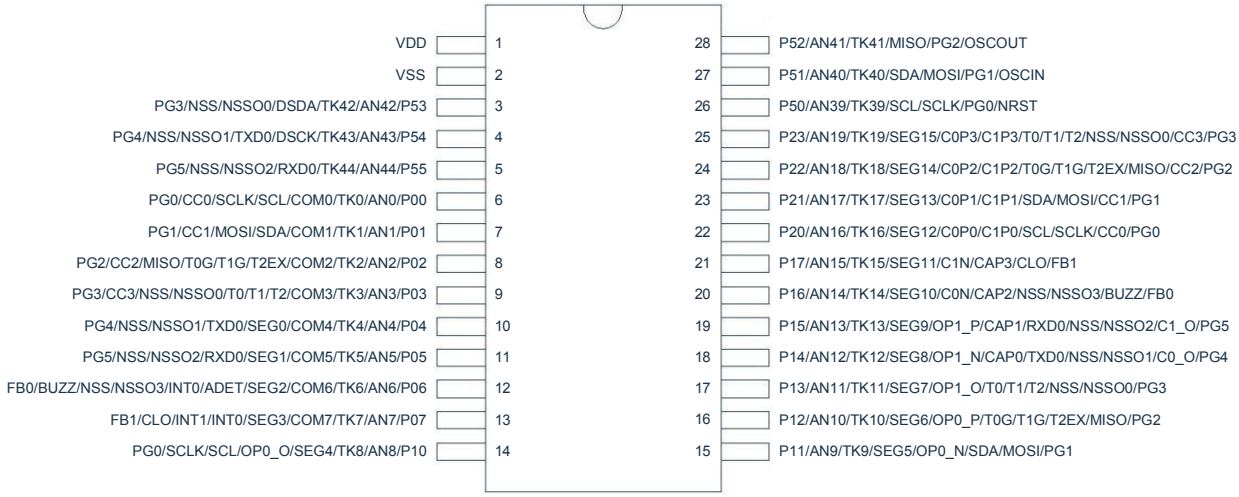
XSFR is a special register shared by the addressing space of XRAM, which mainly includes port control register and other function control registers. Its addressing range is as follows:



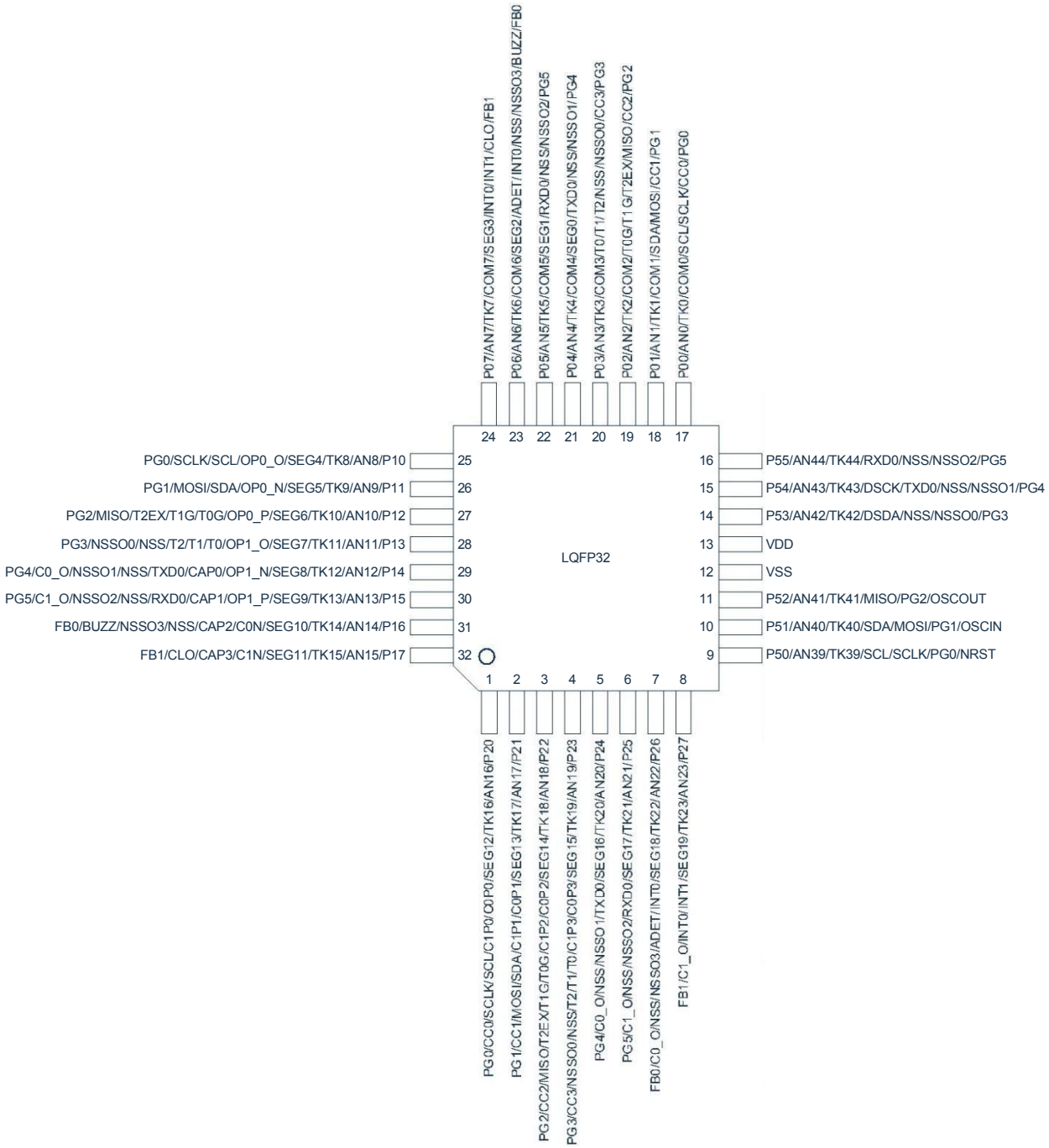
3. Pin Assignment

3.1 Pin Description

3.1.1 CMS80F7518



3.1.2 CMS80F7519



3.2 Pin Description

Symbol description：I/O digital input or output, I digital input, O digital output, AI analog input, AO analog output.

Number		Function	Type	Description
SOP28	LQFP32			
6	17	P00	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN0	AI	ADC channel 0 input
		TK0	AI	Touch button channel 0 input
		COM0	AO/O	LCD/LED COM0 output
		SCL	I/O	I²C clock input and output
		SCLK	I/O	SPI clock input and output
		CC0	O	Timer2 comparison output channel 0
		PG0	O	PWM output channel 0
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
7	18	P01	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN1	AI	ADC channel 1 input
		TK1	AI	Touch button channel 1 input
		COM1	AO/O	LCD/LED COM1 output
		SDA	I/O	I²C data input and output
		MOSI	I/O	SPI master send and slave receive
		CC1	O	Timer2 comparison output channel 1
		PG1	O	PWM output channel 1
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
8	19	P02	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN2	AI	ADC channel 2 input
		TK2	AI	Touch button channel 2 input
		COM2	AO/O	LCD/LED COM2 output
		T0G	I	Timer0 gate control input
		T1G	I	Timer1 gate control input
		T2EX	I	Timer2 fall edge automatic reload input
		MISO	I/O	SPI master receive and slave send
		CC2	O	Timer2 comparison output channel 2
		PG2	O	PWM output channel 2
		TXD1	O	UART1 data output

Number		Function	Type	Description
SOP28	LQFP32			
		RXD1	I/O	UART1 data input or synchronous mode data output
9	20	P03	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN3	AI	ADC channel 3 input
		TK3	AI	Touch button channel 3 input
		COM3	AO/O	LCD/LED COM3 output
		T0	I	Timer0 external clock input
		T1	I	Timer1 external clock input
		T2	I	Timer2 external events or gate control input
		NSS(NSSO0)	I/O	SPI slave select input or master select channel 0 output
		CC3	O	Timer2 comparison output channel 3
		PG3	O	PWM output channel 3
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
10	21	P04	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN4	AI	ADC channel 4 input
		TK4	AI	Touch button channel 4 input
		SEG0	AO/O	LCD/LED SEG0 output
		COM4	AO/O	LCD/LED COM4 output
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	SPI slave select input or master select channel 1 output
		PG4	O	PWM output channel 4
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
11	22	P05	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN5	AI	ADC channel 5 input
		TK5	AI	Touch button channel 5 input
		SEG1	AO/O	LCD/LED SEG1 output
		COM5	AO/O	LCD/LED COM5 output
		RXD0	I/O	UART0 data input or synchronous mode data output

Number		Function	Type	Description
SOP28	LQFP32			
		NSS(NSSO2)	I/O	SPI slave select input or master select channel 2 output
		PG5	O	PWM output channel 5
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
12	23	P06	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN6	AI	ADC channel 6 input
		TK6	AI	Touch button channel 6 input
		SEG2	AO/O	LCD/LED SEG2 output
		COM6	AO/O	LCD/LED COM6 output
		ADET	I	ADC external trigger input
		INT0	I	External interrupt 0 input
		NSS(NSSO3)	I/O	SPI slave select input or master select channel 3 output
		BUZZ	O	Buzzer output
		FB0	I	PWM external brake signal 0 input
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
13	24	P07	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN7	AI	ADC channel 7 input
		TK7	AI	Touch button channel 7 input
		SEG3	AO/O	LCD/LED SEG3 output
		COM7	AO/O	LCD/LED COM7 output
		INT0	I	External interrupt 0 input
		INT1	I	External interrupt 1 input
		CLO	O	System clock division output
		FB1	I	PWM external brake signal 1 input
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
14	25	P10	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN8	AI	ADC channel 8 input
		TK8	AI	Touch button channel 8 input

Number		Function	Type	Description
SOP28	LQFP32			
		SEG4	AO/O	LCD/LED SEG4 output
		OP0_O	AO	OP0 output
		SCL	I/O	I²C clock input and output
		SCLK	I/O	SPI clock input and output
		PG0	O	PWM output channel 0
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
15	26	P11	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN9	AI	ADC channel 9 input
		TK9	AI	Touch button channel 9 input
		SEG5	AO/O	LCD/LED SEG5 output
		OP0_N	AI	OP0 negative channel input
		SDA	I/O	I²C data input and output
		MOSI	I/O	SPI master send and slave receive
		PG1	O	PWM output channel 1
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
16	27	P12	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN10	AI	ADC channel 10 input
		TK10	AI	Touch button channel 10 input
		SEG6	AO/O	LCD/LED SEG6 output
		OP0_P	AI	OP0 positive channel input
		T0G	I	Timer0 gate control input
		T1G	I	Timer1 gate control input
		T2EX	I	Timer2 fall edge automatic reload input
		MISO	I/O	SPI master receive and slave send
		PG2	O	PWM output channel 2
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
17	28	P13	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN11	AI	ADC channel 11 input
		TK11	AI	Touch button channel 11 input

Number		Function	Type	Description
SOP28	LQFP32			
		SEG7	AO/O	LCD/LED SEG7 output
		OP1_O	AO	OP1 output
		T0	I	Timer0 external clock input
		T1	I	Timer1 external clock input
		T2	I	Timer2 external events or gate control input
		NSS(NSSO0)	I/O	SPI slave select input or master select channel 0 output
		PG3	O	PWM output channel 3
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
18	29	P14	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN12	AI	ADC channel 12 input
		TK12	AI	Touch button channel 12 input
		SEG8	AO/O	LCD/LED SEG8 output
		OP1_N	AI	OP1 negative channel input
		CAP0	I	Timer2 input capture channel 0
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	SPI slave select input or master select channel 1 output
		C0_O	O	ACMP0 output
		PG4	O	PWM output channel 4
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
19	30	P15	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN13	AI	ADC channel 13 input
		TK13	AI	Touch button channel 13 input
		SEG9	AO/O	LCD/LED SEG9 output
		OP1_P	AI	OP1 positive channel input
		CAP1	I	Timer2 input capture channel 1
		RXD0	I/O	UART0 data input or synchronous mode data output
		NSS(NSSO2)	I/O	SPI slave select input or master select channel 2 output
		C1_O	O	ACMP1 output

Number		Function	Type	Description
SOP28	LQFP32			
		PG5	O	PWM output channel 5
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
20	31	P16	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN14	AI	ADC channel 14 input
		TK14	AI	Touch button channel 14 input
		SEG10	AO/O	LCD/LED SEG10 output
		C0N	AI	ACMP0 negative input channel
		CAP2	I	Timer2 input capture channel 2
		NSS(NSSO3)	I/O	SPI slave select input or master select channel 3 output
		BUZZ	O	Buzzer output
		FB0	I	PWM external brake signal 0 input
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
21	32	P17	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN15	AI	ADC channel 15 input
		TK15	AI	Touch button channel 15 input
		SEG11	AO/O	LCD/LED SEG11 output
		C1N	AI	ACMP1 negative input channel
		CAP3	I	Timer2 input capture channel 3
		CLO	O	System clock division output
		FB1	I	PWM external brake signal 1 input
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
22	1	P20	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN16	AI	ADC channel 16 input
		TK16	AI	Touch button channel 16 input
		SEG12	AO/O	LCD/LED SEG12 output
		C0P0	AI	ACMP0 positive input channel 0
		C1P0	AI	ACMP1 positive input channel 0
		SCL	I/O	I^2C clock input and output

Number		Function	Type	Description
SOP28	LQFP32			
		SCLK	I/O	SPI clock input and output
		CC0	O	Timer2 comparison output channel 0
		PG0	O	PWM output channel 0
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
23	2	P21	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN17	AI	ADC channel 17 input
		TK17	AI	Touch button channel 17 input
		SEG13	AO/O	LCD/LED SEG13 output
		C0P1	AI	ACMP0 positive input channel 1
		C1P1	AI	ACMP1 positive input channel 1
		SDA	I/O	I^2C data input and output
		MOSI	I/O	SPI master send and slave receive
		CC1	O	Timer2 comparison output channel 1
		PG1	O	PWM output channel 1
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
24	3	P22	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN18	AI	ADC channel 18 input
		TK18	AI	Touch button channel 18 input
		SEG14	AO/O	LCD/LED SEG14 output
		C0P2	AI	ACMP0 positive input channel 2
		C1P2	AI	ACMP1 positive input channel 2
		T0G	I	Timer0 gate control input
		T1G	I	Timer1 gate control input
		T2EX	I	Timer2 fall edge automatic reload input
		MISO	I/O	SPI master receive and slave send
		CC2	O	Timer2 comparison output channel 2
		PG2	O	PWM output channel 2
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
25	4	P23	I/O	GPIO configures input or output, pull-up or pull-down functions through registers

Number		Function	Type	Description
SOP28	LQFP32			
		AN19	AI	ADC channel 19 input
		TK19	AI	Touch button channel 19 input
		SEG15	AO/O	LCD/LED SEG15 output
		C0P3	AI	ACMP0 positive input channel 3
		C1P3	AI	ACMP1 positive input channel 3
		T0	I	Timer0 external clock input
		T1	I	Timer1 external clock input
		T2	I	Timer2 external events or gate control input
		NSS(NSSO0)	I/O	SPI slave select input or master select channel 0 output
		CC3	O	Timer2 comparison output channel 3
		PG3	O	PWM output channel 3
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
--	5	P24	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN20	AI	ADC channel 20 input
		TK20	AI	Touch button channel 20 input
		SEG16	AO/O	LCD/LED SEG16 output
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	SPI slave select input or master select channel 1 output
		C0_O	O	ACMP0 output
		PG4	O	PWM output channel 4
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
--	6	P25	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN21	AI	ADC channel 21 input
		TK21	AI	Touch button channel 21 input
		SEG17	AO/O	LCD/LED SEG17 output
		RXD0	I/O	UART0 data input or synchronous mode data output
		NSS(NSSO2)	I/O	SPI slave select input or master select channel 2 output
		C1_O	O	ACMP1 output

Number		Function	Type	Description
SOP28	LQFP32			
		PG5	O	PWM output channel 5
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
--	7	P26	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN22	AI	ADC channel 22 input
		TK22	AI	Touch button channel 22 input
		SEG18	AO/O	LCD/LED SEG18 output
		ADET	I	ADC external trigger input
		INT0	I	External interrupt 0 input
		NSS(NSSO3)	I/O	SPI slave select input or master select channel 3 output
		C0_O	O	ACMP0 output
		FB0	I	PWM external brake signal 0 input
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
--	8	P27	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN23	AI	ADC channel 23 input
		TK23	AI	Touch button channel 23 input
		SEG19	AO/O	LCD/LED SEG19 output
		INT0	I	External interrupt 0 input
		INT1	I	External interrupt 1 input
		C1_O	O	ACMP1 output
		FB1	I	PWM external brake signal 1 input
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
26	9	P50	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN39	AI	ADC channel 39 input
		TK39	AI	Touch button channel 39 input
		NRST	I	External reset
		SCL	I/O	I^2C clock input and output
		SCLK	I/O	SPI clock input and output
		PG0	O	PWM output channel 0

Number		Function	Type	Description
SOP28	LQFP32			
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
27	10	P51	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN40	AI	ADC channel 40 input
		TK40	AI	Touch button channel 40 input
		OSCIN	AI	External oscillation input
		SDA	I/O	I^2C data input and output
		MOSI	I/O	SPI master send and slave receive
		PG1	O	PWM output channel 1
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
28	11	P52	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN41	AI	ADC channel 41 input
		TK41	AI	Touch button channel 41 input
		OSCOUT	AO	External oscillation output
		MISO	I/O	SPI master receive and slave send
		PG2	O	PWM output channel 2
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
3	14	P53	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN42	AI	ADC channel 42 input
		TK42	AI	Touch button channel 42 input
		DSDA	I/O	Programming and debugging data input and output
		NSS(NSSO0)	I/O	SPI slave select input or master select channel 0 output
		PG3	O	PWM output channel 3
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
4	15	P54	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN43	AI	ADC channel 43 input

Number		Function	Type	Description
SOP28	LQFP32			
		TK43	AI	Touch button channel 43 input
		DSCK	I	Programming and debugging clock input and output
		TXD0	O	UART0 data output
		NSS(NSSO1)	I/O	SPI slave select input or master select channel 1 output
		PG4	O	PWM output channel 4
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
5	16	P55	I/O	GPIO configures input or output, pull-up or pull-down functions through registers
		AN44	AI	ADC channel 44 input
		TK44	AI	Touch button channel 44 input
		RXD0	I/O	UART0 data input or synchronous mode data output
		NSS(NSSO2)	I/O	SPI slave select input or master select channel 2 output
		PG5	O	PWM output channel 5
		TXD1	O	UART1 data output
		RXD1	I/O	UART1 data input or synchronous mode data output
1	13	VDD	P	Power supply
2	12	VSS	P	Ground

3.3 GPIO Features

Various functions of the pins are shared, and each I/O port can be configured as any digital function or specified analog function. As a general-purpose GPIO port, I/O has the following features：

- Configurable 2 levels of I/O output rate.
- Can read data latch status or pin status.
- Configurable rising edge, falling edge, both edge trigger interrupt.
- Configurable rising edge, falling edge, both edge interrupt to wake up the chip.
- Can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 Pin Function List

Digital function list:

	External input	Digital function configuration							
		0	1	2	3	4	5	6	7
P00	-	GPIO	ANA	SCL	SCLK	CC0	PG0	TXD1	RXD1
P01	-	GPIO	ANA	SDA	MOSI	CC1	PG1	TXD1	RXD1
P02	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	PG2	TXD1	RXD1
P03	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	CC3	PG3	TXD1	RXD1
P04	-	GPIO	ANA	TXD0	NSS(NSSO1)	-	PG4	TXD1	RXD1
P05	-	GPIO	ANA	RXD0	NSS(NSSO2)	-	PG5	TXD1	RXD1
P06	ADET/INT0	GPIO	ANA	-	NSS(NSSO3)	BUZZ	FB0	TXD1	RXD1
P07	INT0/INT1	GPIO	ANA	-	-	CLO	FB1	TXD1	RXD1
P10	-	GPIO	ANA	SCL	SCLK	-	PG0	TXD1	RXD1
P11	-	GPIO	ANA	SDA	MOSI	-	PG1	TXD1	RXD1
P12	T0G/T1G/T2EX	GPIO	ANA	-	MISO	-	PG2	TXD1	RXD1
P13	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	-	PG3	TXD1	RXD1
P14	CAP0	GPIO	ANA	TXD0	NSS(NSSO1)	C0_O	PG4	TXD1	RXD1
P15	CAP1	GPIO	ANA	RXD0	NSS(NSSO2)	C1_O	PG5	TXD1	RXD1
P16	CAP2	GPIO	ANA	-	NSS(NSSO3)	BUZZ	FB0	TXD1	RXD1
P17	CAP3	GPIO	ANA	-	-	CLO	FB1	TXD1	RXD1
P20	-	GPIO	ANA	SCL	SCLK	CC0	PG0	TXD1	RXD1
P21	-	GPIO	ANA	SDA	MOSI	CC1	PG1	TXD1	RXD1
P22	T0G/T1G/T2EX	GPIO	ANA	-	MISO	CC2	PG2	TXD1	RXD1
P23	T0/T1/T2	GPIO	ANA	-	NSS(NSSO0)	CC3	PG3	TXD1	RXD1
P24	-	GPIO	ANA	TXD0	NSS(NSSO1)	C0_O	PG4	TXD1	RXD1
P25	-	GPIO	ANA	RXD0	NSS(NSSO2)	C1_O	PG5	TXD1	RXD1
P26	ADET/INT0	GPIO	ANA	-	NSS(NSSO3)	C0_O	FB0	TXD1	RXD1
P27	INT0/INT1	GPIO	ANA	-	-	C1_O	FB1	TXD1	RXD1
P50	NSRT	GPIO	ANA	SCL	SCLK	-	PG0	TXD1	RXD1
P51	-	GPIO	ANA	SDA	MOSI	-	PG1	TXD1	RXD1
P52	-	GPIO	ANA	-	MISO	-	PG2	TXD1	RXD1
P53	-	GPIO	ANA	-	NSS(NSSO0)	-	PG3	TXD1	RXD1
P54	-	GPIO	ANA	TXD0	NSS(NSSO1)	-	PG4	TXD1	RXD1
P55	-	GPIO	ANA	RXD0	NSS(NSSO2)	-	PG5	TXD1	RXD1

Led, analog functions, CONFIG configuration list:

	GPIO(0)		ANA(1)						CONFIG
	LEDSEG	LEDCOM	ADC	TOUCH	LCDSEG	LCDCOM	ACMP	OP	
P00	-	COM0	AN0	TK0	-	COM0	-	-	-
P01	-	COM1	AN1	TK1	-	COM1	-	-	-
P02	-	COM2	AN2	TK2	-	COM2	-	-	-
P03	-	COM3	AN3	TK3	-	COM3	-	-	-
P04	SEG0	COM4	AN4	TK4	SEG0	COM4	-	-	-
P05	SEG1	COM5	AN5	TK5	SEG1	COM5	-	-	-
P06	SEG2	COM6	AN6	TK6	SEG2	COM6	-	-	-
P07	SEG3	COM7	AN7	TK7	SEG3	COM7	-	-	-
P10	SEG4	-	AN8	TK8	SEG4	-	-	OP0_O	-
P11	SEG5	-	AN9	TK9	SEG5	-	-	OP0_N	-
P12	SEG6	-	AN10	TK10	SEG6	-	-	OP0_P	-
P13	SEG7	-	AN11	TK11	SEG7	-	-	OP1_O	-
P14	SEG8	-	AN12	TK12	SEG8	-	-	OP1_N	-
P15	SEG9	-	AN13	TK13	SEG9	-	-	OP1_P	-
P16	SEG10	-	AN14	TK14	SEG10	-	C0N	-	-
P17	SEG11	-	AN15	TK15	SEG11	-	C1N	-	-
P20	SEG12	-	AN16	TK16	SEG12	-	C0P0/C1P0	-	-
P21	SEG13	-	AN17	TK17	SEG13	-	C0P1/C1P1	-	-
P22	SEG14	-	AN18	TK18	SEG14	-	C0P2/C1P2	-	-
P23	SEG15	-	AN19	TK19	SEG15	-	C0P3/C1P3	-	-
P24	SEG16	-	AN20	TK20	SEG16	-	-	-	-
P25	SEG17	-	AN21	TK21	SEG17	-	-	-	-
P26	SEG18	-	AN22	TK22	SEG18	-	-	-	-
P27	SEG19	-	AN23	TK23	SEG19	-	-	-	-
P50	-	-	AN39	TK39	-	-	-	-	NRST
P51	-	-	AN40	TK40	-	-	-	-	OSCIN
P52	-	-	AN41	TK41	-	-	-	-	OSCOUT
P53	-	-	AN42	TK42	-	-	-	-	DSDA
P54	-	-	AN43	TK43	-	-	-	-	DSCK
P55	-	-	AN44	TK44	-	-	-	-	-

Note: 1. The chip pins are subject to the actual chip.

4. Function Summary

4.1 System Clock

The system clock has 4 clock sources, which can be selected through the system configuration register settings. The system clock can be selected from the following 4 types:

- Internal high-speed oscillator HSI (48MHz).
- External high-speed oscillator HSE (8MHz/16MHz).
- External low-speed oscillator LSE (32.768KHz).
- Internal low-speed oscillator LSI (125KHz).

4.2 Reset

The reset operation is used to complete the initialization of the internal circuit of the chip, so that the system starts working from a certain state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low-voltage reset.
- Watchdog overflow reset.
- Software reset.
- CONFIG state protection reset.
- Power-on configuration monitoring reset.

Any of the above reset situations requires a certain response time, and the system provides a complete reset process to ensure the smooth progress of the reset action.

4.3 Power Management

4.3.1 Operating Mode

The chip has 3 different working modes to meet the power consumption requirements of different applications.

- Normal working mode

  MCU is in normal working state and peripherals are operating normally.

- Idle mode

  MCU is in idle mode, CPU stops working, peripherals are operating normally. This mode can be awakened by any interrupt.

- Sleep mode(STOP)

  MCU is in sleep mode, CPU stops working, peripherals stop working. This mode can be awakened by INT0/1, external interrupt, WUT timer, LSE timer.

4.3.2 Power Supply Low-voltage Reset (LVR)

When the power supply voltage is lower than the set detection voltage, the system resets.

There are 4 options for low voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Power Supply Low-voltage Detection (LVD)

The low voltage detection circuit compares the power supply voltage with the set voltage, and if the power supply voltage is lower than the set voltage, an interrupt request signal is generated.

There are 16 options for the settable detection voltage: 2.0V ~ 4.6V.

4.4 Interrupt control

The chip has multiple interrupt sources and interrupt vectors. The user-settable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer, SCM, PWM, I2C, SPI, UART0/1, P0/P1/P2/P5, ACMP0/1, ADC, LVD, TOUCH, the actual number of interrupt sources varies by product.

The chip stipulates two interrupt priority levels, which can realize two-level interrupt nesting. When an interrupt has been responded, if a high-level interrupt sends a request, the latter can interrupt the former to achieve interrupt nesting.

4.5 Timer

4.5.1 Watch Dog Timer (WDT)

The watchdog timer is an on-chip timer whose clock source is provided by the system clock. The WDT timeout will generate a reset. The watchdog reset is a protection setting of the system. When the system runs to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an infinite loop. The WDT timer has the following characteristics:

- 8 levels of watchdog overflow time are selectable.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 Timer Counter 0/1 (Timer0/1)

Timer 0 is similar in type and structure to Timer 1, and is two 16-bit up-counting timers. Timer0 has 4 working modes, Timer1 has 3 working modes, they provide basic timing and event counting operations.

In "timer mode", the timer register is incremented every 12 or 4 system cycles when the timer clock is enabled. In the "counter mode", the timing register will increase whenever it detects a falling edge on the corresponding input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- Can be used for gated counting function.
- Counter overflow interrupt.

4.5.3 Timer Counter 2 (Timer2)

Timer 2 is a 16-bit timer, which can be used for various digital signal generation and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following characteristics:

- Can be used as a normal timer.
- Can be used for gated timing function.
- External counting function can be realized.
- With reload prohibition, overflow auto-reload, external pin falling edge auto-reload function.
- Capture can be triggered by rising edge, falling edge, both edges or writing the low byte of the capture register.
- With a comparison function, this function can generate a periodic signal and a PWM waveform with a controllable duty cycle.
- Interrupts can be generated by timer, external trigger, capture or comparison.

4.5.4 Timer 3/4 (Timer3/4)

Timer 3/4 is similar to timer 0/1 and is two 16-bit timers. Timer3 has 4 working modes, and Timer4 has 3 working modes. Compared with Timer0/1, Timer3/4 only provides timing operation.

When the timer is started, the value of the register (counter) is incremented every 12 or 4 system cycles.

4.5.5 LSE Timer

The LSE timer is a 16-bit up-counting timer with a clock source from the external low-speed clock LSE. The LSE timer has the following characteristics:

- Timing function.
- 16-bit timing value can be set.
- Can work normally in sleep mode.
- An interrupt can be generated when the count value is equal to the timer value.
- Timed interrupt can wake up idle mode 1/idle mode 2/sleep mode.

4.5.6 Wake-up Timer (WUT)

WUT wake-up timer is a 12-bit, up-counting timer used for wake-up from sleep and a clock source from the internal low-speed clock LSI. After the system enters the sleep mode, the CPU and all peripheral circuits stop working, and the internal low-speed clock LSI provides the clock for the WUT counter. WUT has the following characteristics:

- The system can be woken up regularly in sleep mode.
- Count clock can be divided by 1, 8, 32, 256.
- 12-bit timing value can be set.

4.5.7 Baud Rate Timer (BRT)

The BRT timers are 16-bit baud rate timers whose clock source comes from the system clock. They mainly provide clocks for the UART module. BRT has the following characteristics:

- With independent control switch.
- Counting clock has 8 frequency division options.
- 16-bit up counting.

4.6 Enhanced Digital Peripherals

4.6.1 Cyclic Redundancy Check (CRC)

CRC is a commonly used error-detecting code. The main feature is that any choice of length of information data and verification data is possible. CRC verification unit generates polynomial '$X^{16}+X^{12}+X^5+1$'(CRC-16-CCITT). The data that needs to be checked is selected from programs, therefore this module is not only used in program flashspace but many other places.

4.6.2 Multiplication and Division Unit (MDU)

The MDU module has the following characteristics:

- Support 32bit/16bit division.
- Support 16bit/16bit division.
- Support 16bit×16bit multiplication.
- Support 32 bit shift operation.
- Support normalization operation.

4.6.3 BUZZER

The buzzer driver is composed of an 8-bit counter, a clock driver, and a control register. It outputs a square wave with a duty cycle of 50%, and its frequency covers a wide range. BUZZER has the following characteristics:

- With separate enable control switch.
- A total of 4 levels of system clock divider ratios of 8, 16, 32, 64 can be set.
- Output frequency divider can be set (1~255) x 2 through 8-bit register.

4.6.4 Enhanced PWM Module

The enhanced PWM module supports 6 PWM generators, and the period and duty cycle can be set independently. PWM has the following characteristics:

- Support 2 kinds of waveform output in single and continuous mode.
- Support 4 control modes: independent, complementary, synchronous and group control.
- Count clock can be divided by 1, 2, 4, 8, 16.
- Support two counting modes: edge alignment and center alignment, symmetrical and asymmetrical counting are supported in center alignment mode.
- Support mask output.
- Support dead zone programming.
- Output polarity can be set.
- Support cycle, compare up, compare down, zero interrupt.
- Support software brake, external port trigger brake, ADC comparison result trigger brake, ACMP output trigger brake.

4.7 Display Interface

4.7.1 Hardware LCD Driver Module

The LCD drive module includes a controller, a duty cycle generator, COM and SEG output ports. The module has the following characteristics:

- Up to 8 COM ports and 20 SEG ports.
- Support two modes of traditional resistance and fast charging.
- The fast charging time is optional.
- Support contrast adjustment.
- Optional bias voltage: 1/2, 1/3, 1/4.
- The duty cycle is optional: 1/4, 1/5, 1/6, 1/8.
- The clock source is optional: system clock, LSI, LSE.

4.7.2 Hardware LED Drive Module

The LED drive module can easily realize the display drive of the LED. The module has the following characteristics:

- 1/4, 1/5, 1/6, 1/8 four kinds of DUTY are optional.
- System clock, LSI, LSE three clock sources are optional
- 16-bit clock source frequency divider controller.
- Two driving modes of common cathode and common anode for COM port are optional.
- Supports up to 8 COM ports and 20 SEG ports.
- The COM port current 50mA and 150mA are two options (VOL=1.5V@VDD=5V).
- The SEG port current can be selected in 16 levels, and the maximum current can reach 40mA (VOH=3.5V@VDD=5V).

4.8 Communication Module

4.8.1 SPI Module

SPI is a fully configurable SPI master/slave device that allows users to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it can also communicate between processors in a multi-host system. SPI has the following characteristics:

- Full-duplex synchronous serial data transmission.
- Support master/slave mode.
- Support multi-host system.
- System error detection.
- Support speed up to 1/4 of the system clock (FSYS≤24MHz).
- Bit rate generates 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Support four transmission formats.
- Send/receive complete can generate interrupt.

4.8.2 I²C Module

The two-wire bidirectional serial bus controller I2C provides a simple and effective connection method for data exchange between the microprocessor and the I2C bus. The I2C module has the following characteristics:

- Support 4 working methods: master sending, master receiving, slave sending, slave receiving.
- Support 2 transmission speed modes:
  Standard (up to 100Kb/s);
  Fast (up to 400Kb/s).
- Perform arbitration and clock synchronization.
- Support multi-host system.
- The host method supports 7-bit addressing mode and 10-bit addressing mode on the I2C bus (software support).
- The slave method supports 7-bit addressing mode on the I2C bus.
- Allows operation in a wide range of clock frequencies (built-in 8-bit timer).
- An interrupt can be generated when receiving/sending is complete.

4.8.3 UARTn Module

UARTn module contains UART0/ UART1, 2 serial ports with exactly the same function. UARTn has the following characteristics:

- Full-duplex serial port.
- Support synchronous mode.
- Support 8-bit asynchronous transceiver mode with variable baud rate.
- Support 9-bit asynchronous transceiver mode with variable baud rate.
- Baud rate can be generated by Timer1/Timer4/Timer2/BRT module.
- Send/receive complete can generate interrupt.

4.9 Analog Module

4.9.1 Analog to Digital Conversion (ADC)

ADC module is a 12-bit successive approximation analog-to-digital converter. The port analog input signal is connected to the input of the analog-to-digital converter after passing through the multiplexer. The analog-to-digital converter generates a 12-bit binary result according to the input analog signal and saves the result in the ADC result register. ADC has the following characteristics:

- Up to 30 external channels.
- ADC conversion clock has 8 clock frequencies to choose from.
- ADC reference voltage can choose 1.2V/2.0V/2.4V/3.0V/VDD.
- A complete 12-bit conversion requires 18.5 ADC conversion cycles.
- Support external port edge, enhanced PWM trigger ADC conversion.
- Support ADC conversion result comparison output, comparison output can control enhanced PWM brake function.
- Support ADC conversion completion to generate interrupt.

4.9.2 TOUCH Module

The touch module is an integrated circuit designed to realize the touch interface of human body. It can replace the mechanical button to realize the waterproof and dustproof, sealed and isolated, strong and beautiful operation interface. Technical parameters:

- Up to 30 touch channels are optional.
- No external touch capacitance required.
- Effective touch response time is less than 100ms.

4.9.3 Analog Comparator (ACMP0/1)

The comparators ACMP0 and ACMP1 have the following characteristics:

- The positive end supports multiple input ports optional.
- The negative terminal can select port input or internal reference voltage.
- The internal reference voltage divider has a total of 16 gear selections.
- Support output filtering, a total of 11 filter time options.
- Support unilateral and bilateral hysteresis control.
- Hysteresis voltage optional 10/20/60mV.
- Support offset voltage through software trimming.
- The output can be used as an enhanced PWM brake trigger signal.
- Support output change to generate interrupt.

4.9.4 Amplifiers（OP0/1）

The Amplifiers OP0 and OP1 have the following characteristics:

- The positive terminal supports internal 1.2V input
- Support two modes of operational amplifier /comparator
- The output of amplifier can be connected to internal ACMP input
- The output can be connected internally to ADC channel 63 for measurement.
- Support software to adjust offset voltage.

4.9.5 Temperature Sensor (TS)

This series of products contains a temperature sensor, temperature sensor has the following characteristics:

- The temperature range can be measured: -40℃~105℃.
- Support software trimming.
- The output can be measured by ADC.

4.10 FLASH Memory

FLASH memory includes program memory (APROM/BOOT) and non-volatile data memory (Data FLASH), which can be accessed through related special function registers (SFR) to realize IAP function. FLASH memory supports the following operations:

- Byte read operation.
- Byte write operation.
- Page erase operation.

4.11 Unique ID (UID)

Each chip has a 96-bit unique identification number, namely Unique identification. The UID has been set at the factory and cannot be modified by the user.

5. User Configuration

The system configuration register (CONFIG) is the FLASH option of the MCU's initial conditions, and the program cannot access and operate it. The following contents can be set through the system configuration register:

- Watchdog's working method.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Low voltage reset voltage.
- Disable or enable debug mode.
- Oscillation method, prescaler selection.
- Internal high-speed oscillator frequency division selection.
- External reset configuration, port selection.
- Sleep wake-up waiting time.
- APROM/BOOT space.

6. Electrical Characteristics

(TA=25℃, Unless otherwise indicated)

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Power supply voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	200	mA
I_{IO}	Maximum sink current of a single IO	-	50	mA
	Maximum sink current of a single IO（LED_COM）	-	150	mA
	Maximum source current of a single IO	-	40	mA
	Maximum source current of a single IO（LED_SEG）	-	40	mA
	Maximum sink current of all IOs	-	200	mA
	Maximum source current of all IOs	-	120	mA

Note: If the operating conditions of the device exceed the absolute maximum rating range, the device will be permanently damaged. Function is guaranteed only if the device operates within the limits specified in the manual. The absolute maximum rating of chips may affect the reliability of devices.

6.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V, T_A=25℃

Symbol	Parameter	Test condition	Min.	Typ.	Max.	unit
VDD	Operating voltage	F_{SYS}=48MHz, machine cycle=2T F_{SYS}=24MHz, machine cycle=1T F_{SYS}=8MHz~16MHz, machine cycle=1T	2.1	-	5.5	V
		TOUCH	3.5	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals are off machine cycle=2T	-	8	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals are off machine cycle=2T	-	8	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off machine cycle=1T	-	5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off machine cycle=1T	-	5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off machine cycle=1T	-	4	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off machine cycle=1T	-	4	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals are off machine cycle=1T	-	3	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off machine cycle=1T	-	3	-	mA
	IDLE	VDD=5V, F_{SYS}=48MHz, all peripherals are off	-	7	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals are off	-	7	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off	-	4	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off	-	4	-	mA

		VDD=5V, F_{SYS}=16MHz, all peripherals are off	-	3.5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off	-	3.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals are off	-	2.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off	-	2.5	-	mA
I_{SLEEP1}	Sleep current	VDD=3V, All peripherals are off, LSE/LSE timer enable	-	20	-	uA
I_{SLEEP2}	Sleep current	VDD=3V, All peripherals are off, LSI/WUT timer enable	-	7	-	uA
I_{SLEEP3}	Sleep current	VDD=3V, All peripherals are off	-	6	-	uA
I_{LI}	Input leakage	-	-1	-	1	uA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
V_{OL}	Output Low voltage	VDD=5V，I_{OL1}=18mA	-	-	0.4	V
		VDD=5V，I_{OL2}=50mA（LED COM）	-	-	0.4	V
		VDD=3V，I_{OL1}=12mA	-	-	0.4	V
		VDD=3V，I_{OL2}=22mA（LED COM）	-	-	0.4	V
V_{OH}	High output voltage	VDD=5V，I_{OH1}=35mA	3.5	-	-	V
		VDD=5V，I_{OH2}=35mA（LED SEG Max）	3.5	-	-	V
		VDD=5V，I_{OH3}=2.6mA（LED SEG Min）	3.5	-	-	V
		VDD=3V，I_{OH1}=13.5mA	2.1	-	-	V
		VDD=3V，I_{OH2}=13.5mA（LED SEG Max）	2.1	-	-	V
		VDD=3V，I_{OH3}=1mA（LED SEG Min）	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC Electrical Parameters

6.3.1 Power-up and Power-down Time

TA=25℃, Not include 32.768K crystal oscillator start-up time.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External Oscillator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HSE}	Operating voltage	F=8/16MHz, C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz, C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

Symbol	Parameter	Condition	Frequency error range	Min.	Typ.	Max.	Unit
F_{HSI}	Internal high speed oscillator 48MHz	T_A= 25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal low speed oscillator 125KHz	T_A=25℃	±20%	-	125	-	KHz
		T_A=-40℃ to 105℃	±50%	-	125	-	KHz

6.3.4 Low-voltage Reset Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVR1}	Low voltage detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low voltage detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low voltage detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low voltage detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 Low-voltage Detection Electrical Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVD1}	Low voltage detection threshold 2.00V	1.90	2.00	2.10	V
V_{LVD2}	Low voltage detection threshold 2.16V	2.06	2.16	2.26	V
V_{LVD3}	Low voltage detection threshold 2.31V	2.21	2.31	2.41	V
V_{LVD4}	Low voltage detection threshold 2.45V	2.35	2.45	2.55	V
V_{LVD5}	Low voltage detection threshold 2.60V	2.50	2.60	2.70	V
V_{LVD6}	Low voltage detection threshold 2.73V	2.63	2.73	2.83	V
V_{LVD7}	Low voltage detection threshold 2.88V	2.78	2.88	2.98	V
V_{LVD8}	Low voltage detection threshold 2.98V	2.88	2.98	3.08	V
V_{LVD9}	Low voltage detection threshold 3.21V	3.11	3.21	3.31	V
V_{LVD10}	Low voltage detection threshold 3.42V	3.32	3.42	3.52	V
V_{LVD11}	Low voltage detection threshold 3.62V	3.52	3.62	3.72	V
V_{LVD12}	Low voltage detection threshold 3.81V	3.71	3.81	3.91	V
V_{LVD13}	Low voltage detection threshold 4.00V	3.90	4.00	4.10	V
V_{LVD14}	Low voltage detection threshold 4.20V	4.10	4.20	4.30	V
V_{LVD15}	Low voltage detection threshold 4.43V	4.33	4.43	4.53	V
V_{LVD16}	Low voltage detection threshold 4.60V	4.50	4.60	4.70	V

6.4 FLASH Electrical Parameter

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	25	105	℃
$N_{ENDURANCE}$	Number of erasing and writing	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	Cycle
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	1.5	-	ms
T_{WRITE}	Write time	-	-	30	-	us
T_{READ}	Read time	-	-	3*Tsys	-	-
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

6.5 Analog Characteristics

6.5.1 BANDGAP Electrical Characteristics

TA=25℃

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{BG}	Internal 1.2V	VDD=2.1~5.5V、T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V、T_A=-20℃ to 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V、T_A=-40℃ to 105℃	1.176	1.2	1.224	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	V_{AVDD}	-	V
V_{REF2}	Reference voltage 2（not V_{BG}）		1.185	1.2	1.215	V
V_{REF3}	Reference voltage 3		1.985	2.0	2.015	V
V_{REF4}	Reference voltage 4		2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	Resolution			12		Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)			±2		LSB
INL	Integral nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us)			±4		LSB
T_{ADCK}	ADC clock cycle	V_{REF}=VDD=5V	0.5	-	-	us
		V_{REF}=V_{REF2}	32	-	-	us
		V_{REF} =V_{REF3}/ V_{REF4}/V_{REF5}	2	-	-	us
I_{ADC}	ADC conversion time		-	18.5	-	T_{ADCK}
F_S	Sampling rate (V_{REF}=V_{AVDD}=5V)			100		Ksps

Note: V_{REF} =$V_{REF2,}$ resolution is 8bit.

6.5.3 ACMP Electrical Characteristics

T_A=25℃, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS0}	ACMP0 Input offset voltage	No calibration (C0CON1[4:0] =10H)	-	±4.0	-	mV
		After calibration	-	±0.5	±1.0	
V_{OS1}	ACMP1 Input offset voltage	-	-	±4.0	-	mV
V_{CM}	Common-mode input range	-40℃ ~105℃	-0.1	-	VDD-1.3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output characteristics						
V_{OH}	Maximum output voltage	-40℃ ~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃ ~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open-loop voltage gain	-	-	90	-	dB
BW	Bandwidth	-	-	200	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V -40℃ ~105℃	-	100	-	dB
Transient characteristics						
T_{STB}	Stable time	-	-	-	5	us
T_{PGD}	Response delay time	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

Note: Design guarantee.

6.5.4 OP Electrical Characteristics

T_A=25℃，V_{SENSE}=V_{IN+}-V_{IN-}，VDD=5V，V_{IN+}=1V，Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply voltage	-	2.5	-	5.5	V
I_Q	Quiescent Current	V_{SENSE}=0mV	-	1.0	1.6	mA
I_{SD}	Shutdown current	-	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input characteristics						
V_{OS}	Input Offset Voltage	NO calibration（OPnCON1[4:0]=10H）	-	±3.5	-	mV
		After calibration	-	±0.5	±1.0	
V_{CM}	Common-mode Input Range	-40℃~105℃	0	-	VDD-1.3	V
I_B	Input Bias Current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset Current	V_{SENSE}=0mV	-	10	-	pA
Output characteristics						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃，I_{LOAD}=0.1mA	-	-	VDD-0.1	V
		-40℃~105℃，I_{LOAD}=1mA	-	-	VDD-0.3	
V_{OL}	Minimum output voltage	-40℃~105℃，I_{LOAD}=0.1mA	0.1	-	-	V
		-40℃~105℃，I_{LOAD}=1mA	0.3	-	-	
Frequency characteristics						
A_{OL}	Open-loop voltage gain	-	-	80	-	dB
BW	Bandwidth	R_{LOAD}=2K,C_{LOAD}=100pF	-	5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	75	-	dB
CMRR	Common mode rejection ratio	V_{IN+}=0.3~（VDD-1.5）℃ -40℃~105	-	90	-	dB
Transient characteristics						
SR	Slew Rate	R_{LOAD} =2K,C_{LOAD} =100pF	-	±8	-	V/μs
T_{STB}	Stable Time	-	-	-	2	μs

Note: Design guarantee.

6.5.5 LCD Driver Electrical Characteristics

TA＝25℃，VDD=2.5V-5.5V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{LCD}	LCD voltage	LCDEN=1,LCDTEN=0		TYP*0.95	VDD	TYP*1.05	V
		LCDEN=1,LCDTEN=1 V_{LCD}=VDD*(15+LCDTVS<3:0>)/30 (LCDTVS<3:0>=0000~1110)		TYP*0.95	V_{LCD}	TYP*1.05	V
V_{BIAS}	LCD bias voltage, DC, no load	1/2 Bias	V_{LC1}	-	(1/2)*V_{LCD}	-	V
		1/3 Bias	V_{LC1}	-	(2/3)*V_{LCD}	-	
			V_{LC2}	-	(1/3)*V_{LCD}	-	
		1/4 Bias	V_{LC1}	-	(3/4)*V_{LCD}	-	
			V_{LC2}	-	(2/4)*V_{LCD}	-	
			V_{LC3}	-	(1/4)*V_{LCD}	-	
I_{LCD}	LCD current	LCDTEN=0	R_{LCD1}=60KΩ	-	80	100	uA
			R_{LCD2}=225KΩ	-	22	27	
			R_{LCD3}=900KΩ	-	5	7	
		LCDTEN=1	LVDTVS<3:0>=1110, R_{LCD1}=60KΩ (Max)	-	185	300	
			LVDTVS<3:0>=0000, R_{LCD3}=225KΩ	-	120	200	
			LVDTVS<3:0>=0000, R_{LCD3}=900KΩ (Min)	-	100	180	
R_{LCD1}	Select resistance 1	LCDRM<1:0>=00		40	60	80	KΩ
R_{LCD2}	Select resistance 2	LCDRM<1:0>=01		160	225	290	
R_{LCD3}	Select resistance 3	LCDRM<1:0>=1x		600	900	1200	

6.5.6 Temperature Sensor Electrical Characteristics

VDD＝5V。

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LINE}	Linearity	-	-	±4	-	℃
K_{AVG}	Slope	-40℃~105℃	3.3	3.5	3.7	mV/℃
V_{25}	25℃ output voltage	T_A＝25℃	0.99	1	1.01	V
T_S	Establishment time	-	-	-	10	us
T_{SMP}	ADC sampling time	-	150	-	-	us

Note: Design guarantee.

6.6 EMC Characteristics

6.6.1 EFT Electrical Characteristics

Symbol	Parameter	Condition	Max.	Unit	Rank
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDD and VSS pins to induce a functional disturbance	T_A = +25°C, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4800	V	4B

Note: The electrical fast transient burst (EFT) immunity performance is closely related to system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.) The EFT parameters in the above table are the results measured on the internal test platform of the CMS, and are not applicable to all application environments. The test data is only for reference. All aspects of system design may affect the EFT performance. In applications with high EFT performance requirements, attention should be paid to avoid interference sources affecting the system operation as much as possible. It is recommended to analyze the interference path and optimize the design to achieve the best anti-interference performance.

6.6.2 ESD Electrical Characteristics

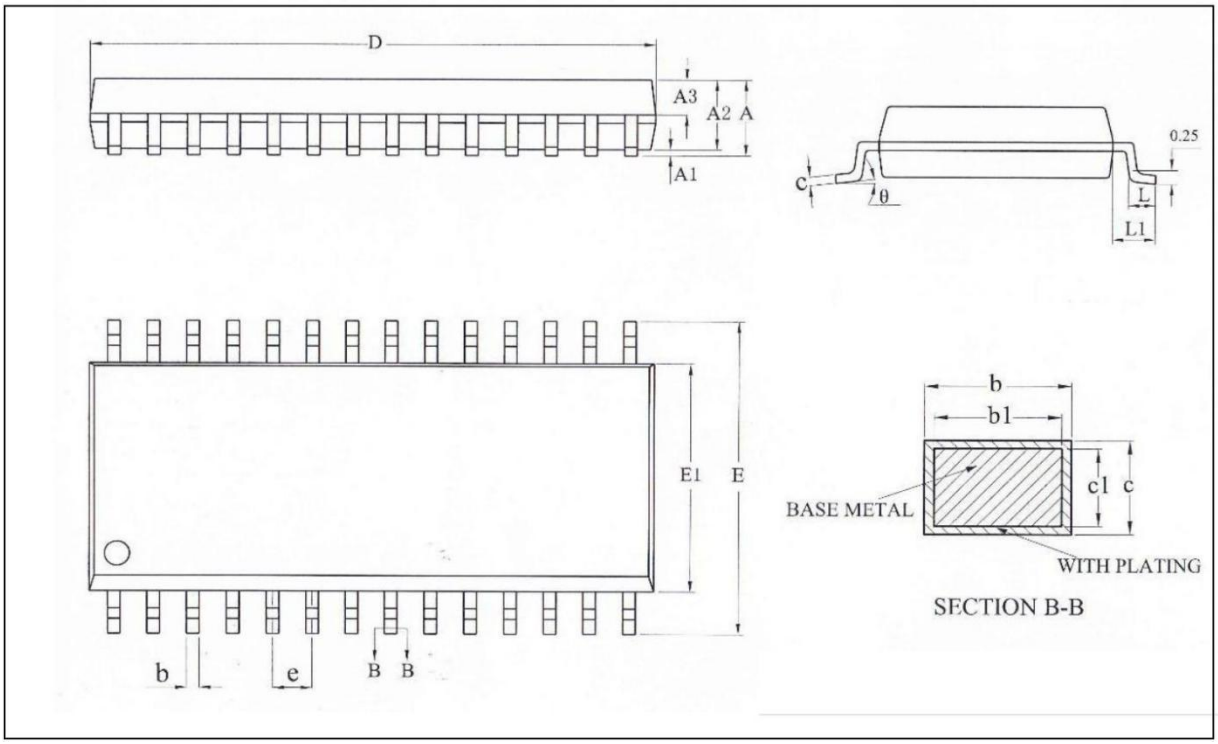
Symbol	Parameter	Condition	Max.	Unit	Rank
V_{ESD}	Electrostatic discharge (Human body discharge mode - HBM)	T_A = + 25°C, JEDEC EIA/JESD22- A114	8000	V	3B
	Electrostatic discharge (Machine discharge mode - MM)	T_A = + 25°C, JEDEC EIA/JESD22- A115	400	V	C

6.6.3 Latch-up Electrical Characteristics

Symbol	Parameter	Condition	Class	Min.	Unit
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25°C)	±200	mA

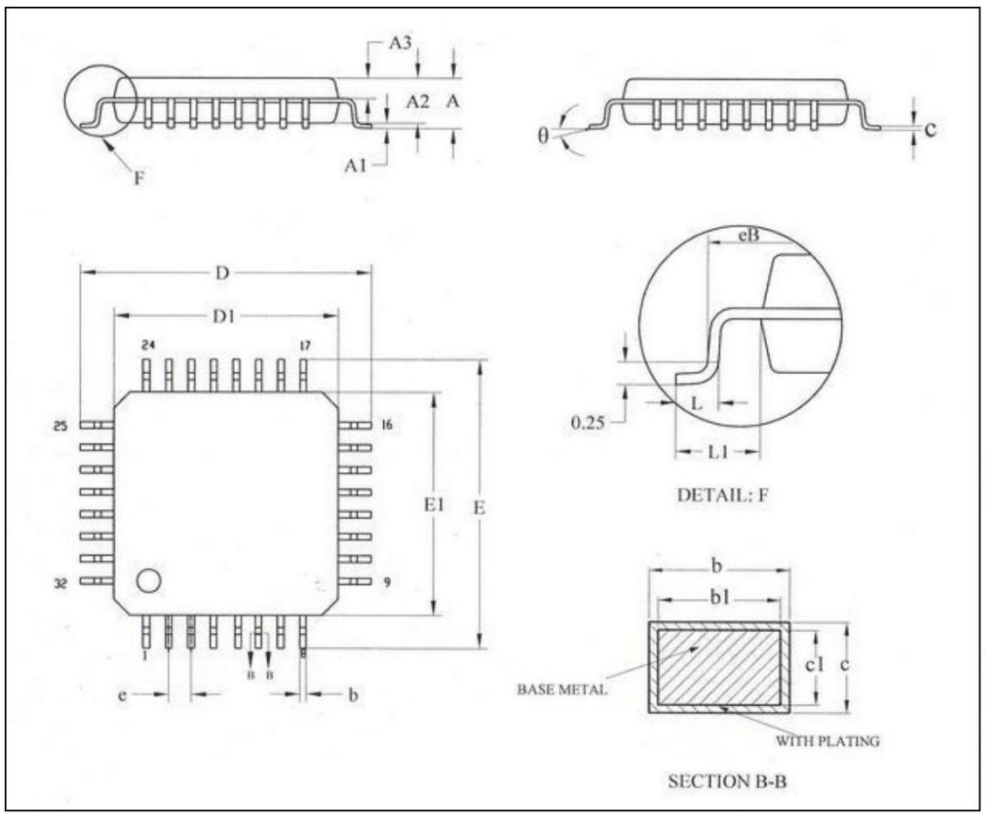
7. Package Information

7.1 SOP28



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0	-	8°

7.2 LQFP32



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

8. Revision History

Revision version	Date	Modify content
V1.00	Oct 2019	Initial version
V1.01	Jan 2020	Modify ADC/FLASH and other electrical parameters
V1.02	Aug 2020	Updated manual format in August 2020
V1.03	Dec 2020	Increase the working voltage of touch buttons
V1.04	Nov 2021	FLASH electrical parameters are corrected
V1.05	Apr 2022	1) 6.1 Absolute Maximum Ratings: Add notes for limit parameters 2) 6.2 DC Electrical Characteristics: Modify the electrical characteristics 3) 6.3.3 Internal Oscillator: modify parameters 4) 6.4 FLASH Electrical Parameter: optimization parameters 5) 6.5.1 BANDGAP Electrical Characteristics: adjust parameters 6) 6.5.2 ADC Electrical Characteristics: the ADC clock cycle is described according to different reference voltages 7) 6.5.4 OP Electrical Characteristics: modify the electrical characteristics and add notes
V1.06	April 2022	1) 6.2 DC Electrical Characteristics: correct parameters 2) 6.5.3 ACMP Electrical Characteristics: adjust parameters 3) 6.5.6 Temperature Sensor Electrical Characteristics: add comments