CMS8S78xx Data Sheet

Enhanced flash 8-bit 1T 8051 microcontroller

Rev. 1.04

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1. Product features

1.1 Features

- **Compatible with mcS-51's 1T command system**
  - The system clock frequency supports up to 48 MHz
  - The machine cycle is supported up to $1T_{SYS}$ @ F_{SYS}≤24MHz
  - The fastest machine cycle supports $2T_{SYS}$ @ F_{SYS}= 48MHz
- **memory**
  - Program FLASH: 16K×8Bit
  - Data FLASH：1K×8Bit
  - General RAM: 256×8Bit
  - Universal XRAM: 1K×8Bit
  - Support BOOT region, 1K/2K/4K optional
  - The program FLASH supports partition protection
- **4 oscillation modes**
  - HSI - Internal high-speed oscillation: 48MHz
  - HSE-External high-speed oscillation: 8MHz/16MHz
  - LSE-External low-speed oscillation: 32.768KHz
  - LSI-Internal low-speed oscillation: 125KHz
- **GPIO**
  - Up to 26 GPIOs
  - Both support pull-up/down resistor function
  - Both support edge (rising/falling/double-edge) interrupts
  - Both support wake-up function
- **Interrupt source**
  - All external port interrupts are supported
  - 7 timer interrupts
  - Other peripheral interrupts
- **timer**
  - WDT Timer (Watchdog Timer)
  - Timer0/1，Timer2，Timer3/4
  - LSE_Timer (supports sleep wake-up function).
  - WUT (wake-up timer)
  - BRT (Serial Port Baud Rate Timer)
- **Buzzer driver**
  - 50% duty cycle, frequency can be set freely
- **Enhanced PWM**
  - 4-channel enhanced PWM
  - 4 mutually independent cycle counters
  - Supports independent/complementary/synchronous/grouped modes
  - Edge alignment/center alignment is supported
  - Supports complementary mode dead-zone delay function
  - Support brake function and brake recovery function
- **Operating voltage range**
  - 2.1V~5.5V
- **Operating temperature range**
  - -40℃~105℃
- **Low Voltage Reset Function (LVR)**
  - 1.8V/2.0V/2.5V/3.5V
- **Low Voltage Detection Function (LVD)**
  - 2.0V~4.6V 16 levels selectable
- **Built-in Temperature Sensor (TS)**
- **High Precision 12-bit ADC**
  - Up to 26 AD external channels
  - Reference Voltage Selectable (1.2V/2.0V/2.4V/3.0V/VDD)
  - detectable Internal 1.2V reference voltage
  - Supports hardware-triggered start conversion features
  - Supports a set of result number comparison functions
- **Support software LCD driver**
  - Software driver 1/3 bias
  - Supports up to 24COM or 24SEG
- **Support software LED driver**
  - COM SEG drive current selectable
  - Supports up to 24COM or 24SEG
- **Two Analog Comparators (ACMP0/1)**
  - 4 options are available on the positive side and internal 1.2V/VDD divider on the negative side
  - The comparator supports unilateral/bilateral hysteresis
  - The internal 1.2V/VDD divider on the negative side can be connected to the internal ADC channel
- **Low-power mode**
  - Idle mode (IDLE)
  - Sleep Mode (STOP)
- **Supports 96-bit unique ID number (UID)**
  - Each chip has a separate ID number
- **Supports two-wire serial programming and debugging**
- **Communication module**
  - 1xSPI (communication rate up to 6Mb/s)
  - 1xI2C (communication rate up to 400Kb/s)
  - 1xUART (baud rate up to 1Mb/s).

1.2 Product Comparison

Product / Peripheral interface		CMS8S7885（24PIN）	CMS8S7895（28PIN）
Maximum clock frequency		48MHz	
Storage Module	APROM	16/15/14/12 KB(1)	
	BOOT	0/1/2/4 KB(1)	
	Data FLASH	1 KB	
	RAM	256 B	
	XRAM	1 KB	
timer	WDT	1	
	Timer0/1	2 (16bit)	
	Timer2	1 (16bit)	
	Timer3/4	2 (16bit)	
	LSE_Timer	1 (16bit)	
	WUT	1 (12bit)	
	BRT	1 (16bit)	
Enhanced Digital peripherals	BUZZER	1	
	PWM	4(16bit)	
Displays the interface	LCD	20COM 20SEG	24COM 24SEG
	LED	20COM 20SEG	24COM 24SEG
Communication module	SPI	1	
	I2C	1	
	UART	1	
Analog module	12bit-ADC (number of external channels).	22	26
	ACMP	2	
GPIOs		22	26
LVR		1.8V/2.0V/2.5V/3.5V	
LVD		2.0 to 4.6 V, 16 levels	
Operating voltage		2.1~5.5 V	
Operating temperature		-40~105 ℃	
packaging		SSOP24	SSOP28

Note: (1) The SIZE OF THE APROM and BOOT SPACE IS SET THROUGH THE SYSTEM CONFIGURATION REGISTER, AND THE TOTAL MAXIMUM APROM AND BOOT SPACE IS 16K.

2. System Overview

2.1 System Introduction

The series is an 8051 core, MCS-51-compatible 1T command system, a general-purpose IO type 8-bit chip, operating at up to 48MHz, the MCU has the following features:

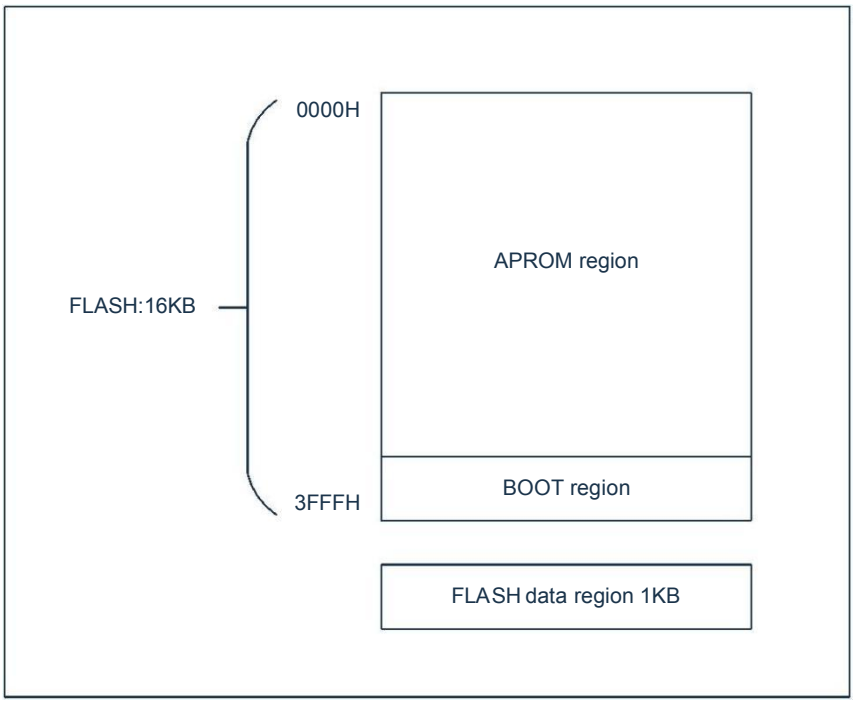
- Features a maximum of 16KB of program area, 256B of RAM space, 1KB of XRAM, and 1KB of non-volatile data area.
- With four oscillation modes, the system clock can be switched freely between the four clock sources, and the external oscillator stop detection.
- Support normal, idle, sleep three working modes, can effectively reduce power consumption.
- Built-in low-voltage reset LVR, low-voltage monitoring LVD, watchdog overflow reset and other protection settings can effectively improve the reliability of system operation.
- It has a variety of interrupt sources such as external interrupts, timer interrupts and other peripheral interrupts, which can respond to external events in a timely manner and improve the utilization of MCUs.
- 9 timers, can achieve timing, counting, input capture, output comparison, timed wake-up, baud rate generator and other functions.
- Supports up to 24COM and 24SEG LED drives
- Supports up to 24COM and 24SEG LCD drives
- 4 channels of 16-bit PWM, support independent, complementary, synchronous three modes of output, with hardware brake function and brake recovery, dead zone control function, mask output and other functions.
- With 1 I2C, 1 SPI, 1 UART communication module, it can realize data transmission between the system and other devices.
- Features a high accuracy 12-bit ADC with selectable internal reference voltage, up to 2 comparators, built-in temperature sensors, and richer analog functions.

2.2 Memory Structure

2.2.1 Program Memory FLASH

The chip has a 16KB flash storage space, and the APROM area and the BOOT area share the entire FLASH space.

The flash space allocation block diagram is as follows:

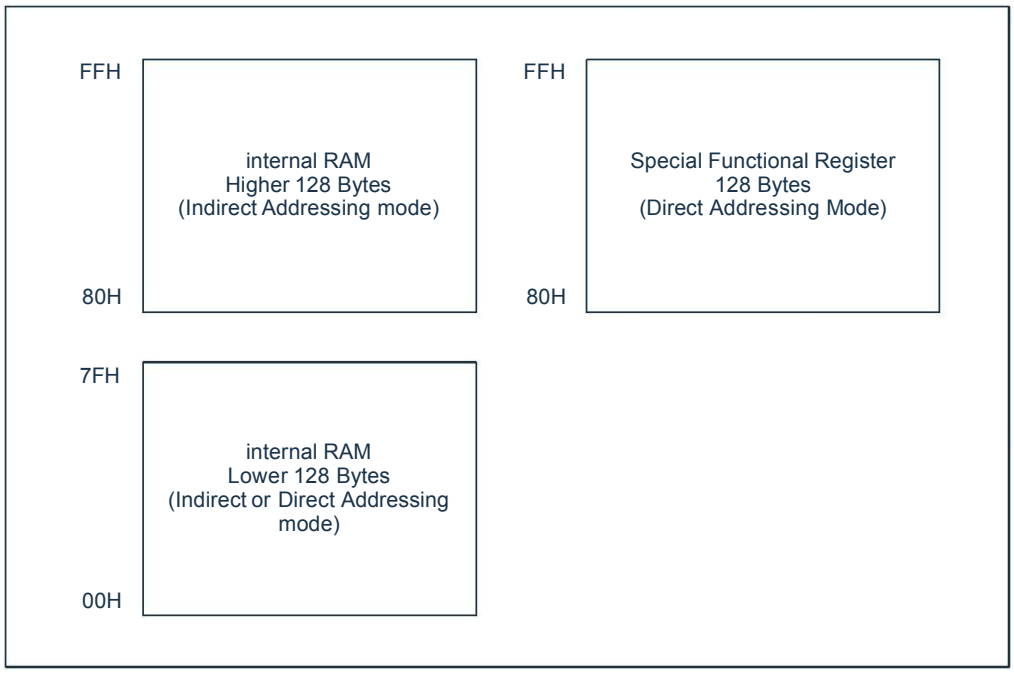


The size of the BOOT can be configured as follows:

16K (program storage area).				
Address space allocation	APROM area		BOOT area	
Mode 0	16K	0000H-3 FFFH	--	--
Mode 1	15K	0000H-3 BFFH	1K	3C00H-3FFFH
Mode 2	14K	0000H-37FFH	2K	3800H-3FFFH
Mode 3	12K	0000H-2 FFFH	4K	3000H-3FFFH

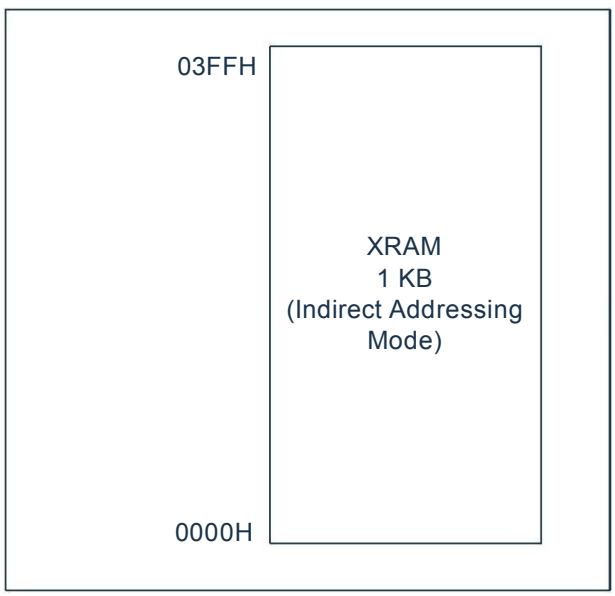
2.2.2 Internal data memory RAM

The internal data memory is divided into 3 parts: low 128Bytes, high 128Bytes, SFR. The RAM space allocation block diagram is shown in the following figure:



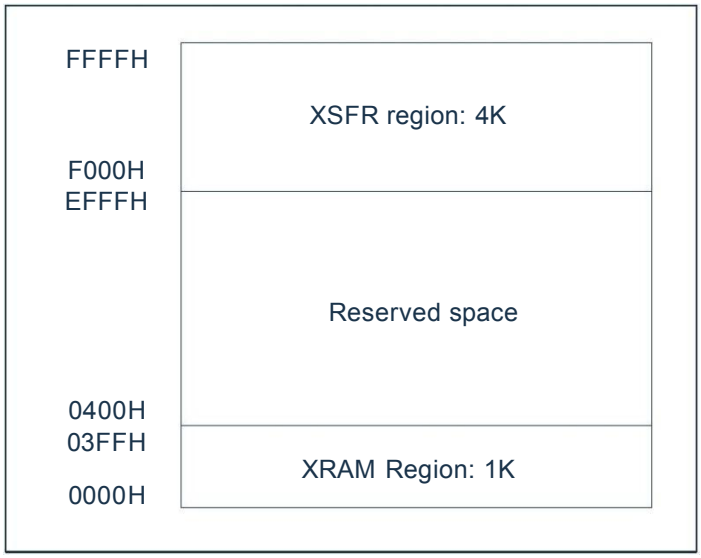
2.2.3 External data memory XRAM

There is a 1KB XRAM area inside the chip, which is not connected to RAM/FLASH, and the XRAM space allocation block diagram is shown in the following figure.



2.2.4 Special function register XSFR

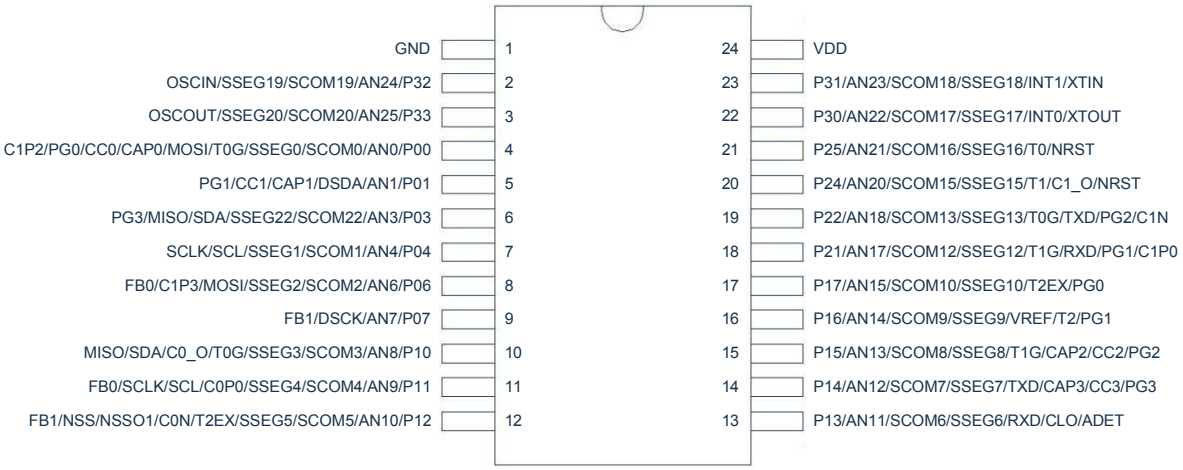
XSFR is a special register shared by the addressing space and XRAM, mainly including: port control registers, other function control registers. Its addressing range is as follows:



3. Pin Definition

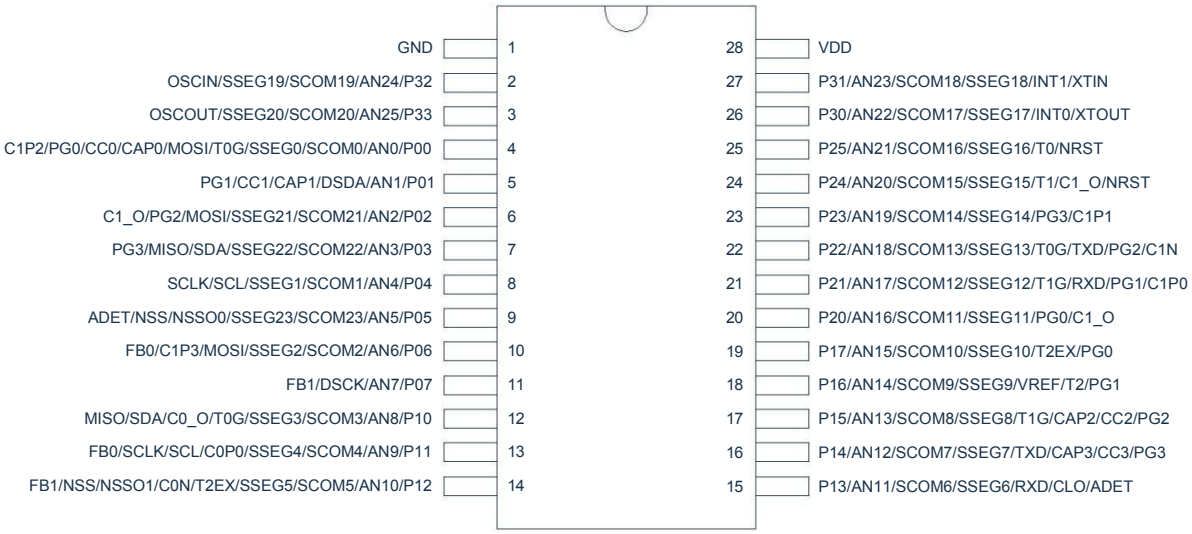
3.1 Pin Description

3.1.1 CMS8S7885 Pin Diagram



CMS8S7885

3.1.2 CMS8S7895 Pin Diagram



CMS8S7895

3.2 Pin function description

Symbol description: I/O represents digital input/output, I represents digital input, O represents digital output, AI represents analog input, and AO represents analog output.

Pin number		Pin name	Pin type	description
SSOP24	SSOP28			
4	4	P00	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN0	AI	ADC channel 0 input
		SCOM0	OSCOUT	LCD/LED COM0 output
		SSEG0	AO/O	LCD/LED SEG0 output
		T0G	I	Timer0 gated input
		MOSI	I/O	SPI data master sends slave receive
		CAP0	I	Timer2 input capture channel 0
		CC0	O	Timer2 compare output channel 0
		PG0	O	PWM channel 0 output
		C1P2	AI	Comparator 1 positive channel 2 input
5	5	P01	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN1	AI	ADC channel 1 input
		DSDA	I/O	Programming/debugging data input and output
		CAP1	I	Timer2 input capture channel 1
		CC1	O	Timer2 compare output channel 1
		PG1	O	PWM channel 1 output
--	6	P02	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN2	AI	ADC channel 2 input
		SCOM21	AO/O	LCD/LED COM21 output
		SSEG21	AO/O	LCD/LED SEG21 output
		MOSI	I/O	SPI data master sends slave receive
		PG2	O	PWM channel 2 output
		C1_O	O	Comparator 1 output
6	7	P03	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN3	AI	ADC channel 3 input
		SCOM22	AO/O	LCD/LED COM22 output
		SSEG22	AO/O	LCD/LED SEG22 output
		SDA	I/O	I2C data input and output
		MISO	I/O	The SPI data master receives the slave send
		PG3	O	PWM channel 3 output
7	8	P04	I/O	GPIO configure input and output through registers, pull

Pin number		Pin name	Pin type	description
SSOP24	SSOP28			
				up, pull down and other functions
		AN4	AI	ADC channel 4 input
		SCOM1	AO/O	LCD/LED COM1 output
		SSEG1	AO/O	LCD/LED SEG1 output
		SCL	I/O	I2C clock input and output
		SCLK	I/O	SPI clock input and output
--	9	P05	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN5	AI	ADC channel 5 input
		SCOM23	AO/O	LCD/LED COM23 output
		SSEG23	AO/O	LCD/LED SEG23 output
		NSS(NSSO0)	I/O	The SPI selects input from the control/main control select 0 output
		AIT	I	ADC external trigger input
8	10	P06	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN6	AI	ADC channel 6 input
		SCOM2	AO/O	LCD/LED COM2 output
		SSEG2	AO/O	LCD/LED SEG2 output
		MOSI	I/O	SPI data master sends slave receive
		C1P3	AI	Comparator 1 positive channel 3 input
		FB0	I	PWM external brake signal 0 input
9	11	P07	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN7	AI	ADC channel 7 input
		DSCK	I	Programming/debugging clock inputs
		FB1	I	PWM external brake signal 1 input
10	12	P10	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN8	AI	ADC channel 8 input
		SCOM3	AO/O	LCD/LED COM3 output
		SSEG3	AO/O	LCD/LED SEG3 output
		T0G	I	Timer0 gated input
		C0_O	O	Comparator 0 output
		SDA	I/O	I2C data input and output
		MISO	I/O	The SPI data master receives the slave send
11	13	P11	I/O	GPIO configure input and output through registers, pull up, pull down and other functions

Pin number		Pin name	Pin type	description
SSOP24	SSOP28			
		AN9	AI	ADC channel 9 input
		SCOM4	AO/O	LCD/LED COM4 output
		SSEG4	AO/O	LCD/LED SEG4 output
		C0P0	AI	Comparator 0 positive channel 0 input
		SCL	I/O	I2C clock input and output
		SCLK	I/O	SPI clock input and output
		FB0	I	PWM external brake signal 0 input
12	14	P12	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN10	AI	ADC channel 10 input
		SCOM5	AO/O	LCD/LED COM5 output
		SSEG5	AO/O	LCD/LED SEG5 output
		T2EX	I	Timer2 drops along the auto-reload input
		C0N	AI	Comparator 0 negative channel input
		NSS(NSSO1)	I/O	The SPI is selected from the control select input/master select 1 output
		FB1	I	PWM external brake signal 1 input
13	15	P13	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN11	AI	ADC channel 11 input
		SCOM6	AO/O	LCD/LED COM6 output
		SSEG6	AO/O	LCD/LED SEG6 output
		RXD	I/O	UART data input/synchronous mode data output
		CLO	O	System clock divider output
		AIT	I	ADC external trigger input
14	16	P14	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN12	AI	ADC channel 12 input
		SCOM7	AO/O	LCD/LED COM7 output
		SSEG7	AO/O	LCD/LED SEG7 output
		TXD	O	UART data output
		CAP3	I	Timer2 input capture channel 3
		CC3	O	Timer2 compare output channel 3
		PG3	O	PWM channel 3 output
15	17	P15	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN13	AI	ADC channel 13 input
		SCOM8	AO/O	LCD/LED COM8 output

Pin number		Pin name	Pin type	description
SSOP24	SSOP28			
		SSEG8	AO/O	LCD/LED SEG8 output
		T1G	I	Timer1 gated input
		CAP2	I	Timer2 input capture channel 2
		CC2	O	Timer2 compare output channel 2
		PG2	O	PWM channel 2 output
16	18	P16	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN14	AI	ADC channel 14 inputs
		SCOM9	AO/O	LCD/LED COM9 output
		SSEG9	AO/O	LCD/LED SEG9 output
		VREF	TheO	Reference voltage output
		T2	I	Timer2 external event or gated input
		PG1	O	PWM channel 1 output
17	19	P17	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN15	AI	ADC channel 15 input
		SCOM10	AO/O	LCD/LED COM10 output
		SSEG10	AO/O	LCD/LED SEG10 output
		T2EX	I	Timer2 drops along the auto-reload input
		PG0	O	PWM channel 0 output
--	20	P20	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN16	AI	ADC channel 16 inputs
		SCOM11	AO/O	LCD/LED COM11 output
		SSEG11	AO/O	LCD/LED SEG11 output
		PG0	O	PWM channel 0 output
		C1_O	O	Comparator 1 output
18	21	P21	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN17	AI	ADC channel 17 input
		SCOM12	AO/O	LCD/LED COM12 output
		SSEG12	AO/O	LCD/LED SEG12 output
2		T1G	I	Timer1 gated input
		RXD	I/O	UART data input/synchronous mode data output
		PG1	O	PWM channel 1 output
		C1P0	AI	Comparator 1 positive channel 0 input
19	22	P22	I/O	GPIO configure input and output through registers, pull up, pull down and other functions

Pin number		Pin name	Pin type	description
SSOP24	SSOP28			
		AN18	AI	ADC channel 18 input
		SCOM13	AO/O	LCD/LED COM13 output
		SSEG13	AO/O	LCD/LED SEG13 output
		T0G	I	Timer0 gated input
		TXD	O	UART data output
		PG2	O	PWM channel 2 output
		C1N	AI	Comparator 1 negative channel input
--	23	P23	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN19	AI	ADC channel 19 input
		SCOM14	AO/O	LCD/LED COM14 output
		SSEG14	AO/O	LCD/LED SEG14 output
		PG3	O	PWM channel 3 output
		C1P1	AI	Comparator 1 positive channel 1 input
20	24	P24	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN20	AI	ADC channel 20 input
		SCOM15	AO/O	LCD/LED COM15 output
		SSEG15	AO/O	LCD/LED SEG15 output
		T1	I	Timer1 external clock input
		C1_O	O	Comparator 1 output
		NRST	I	External reset input
21	25	P25	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN21	AI	ADC channel 21 input
		SCOM16	AO/O	LCD/LED COM16 output
		SSEG16	AO/O	LCD/LED SEG16 output
		T0	I	Timer0 external clock input
		NRST	I	External reset input
22	26	P30	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN22	AI	ADC channel 22 input
		SCOM17	AO/O	LCD/LED COM17 output
		SSEG17	AO/O	LCD/LED SEG17 output
		INT0	I	External interrupt 0 input
		XTOUT	AI	External oscillating LSE output
23	27	P31	I/O	GPIO configure input and output through registers, pull up, pull down and other functions

Pin number		Pin name	Pin type	description
SSOP24	SSOP28			
		AN23	AI	ADC channel 23 input
		SCOM18	AO/O	LCD/LED COM18 output
		SSEG18	AO/O	LCD/LED SEG18 output
		INT1	I	External interrupt 1 input
		XTIN	AI	External oscillating LSE input
2	2	P32	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN24	AI	ADC channel 24 input
		SCOM19	AO/O	LCD/LED COM19 output
		SSEG19	AO/O	LCD/LED SEG19 output
		OSCIN	AI	External oscillation HSE input
3	3	P33	I/O	GPIO configure input and output through registers, pull up, pull down and other functions
		AN25	AI	ADC channel 25 input
		SCOM20	AO/O	LCD/LED COM20 output
		SSEG20	AO/O	LCD/LED SEG20 output
		OSCOUT	AO	External oscillation HSE output
24	28	power supply	P	Supply voltage input pin
1	1	power supply	P	Grounding feet

3.3 GPIO Features

Pins are shared in a variety of functions, and each I/O port can be flexibly configured with digital functions or specified analog functions. I/O as a universal GPIO port has the following characteristics:

- 2 levels I/O output slope can be configured.
- Data latch status or pin status can be read.
- Configurable rising, falling, and dual edge trigger interrupts.
- Configurable rising, falling, and dual-edge interrupt wake-up chip.
- It can be configured as normal input, pull-up input, pull-down input, push-pull output, open-drain output mode.

3.4 List of pin functions

List of digital function ports:

	External input	Digital function configuration							
		0	1	2	3	4	5	6	7
P00	T0G/CAP0	GPIO	ANA	MOSI	-	PG0	CC0	-	-
P01	CAP1	GPIO	ANA	-	-	PG1	CC1	-	-
P02	-	GPIO	ANA	MOSI	-	PG2	C1_O	-	-
P03	-	GPIO	ANA	MISO	SDA	PG3	BUZZ	-	-
P04	-	GPIO	ANA	SCK	SCL	-	-	-	-
P05	CUSTOM	GPIO	ANA	NSS（SSO0）	-	-	-	-	-
P06	-	GPIO	ANA	MOSI	-	FB0	-	-	-
P07	-	GPIO	ANA	-	-	FB1	-	-	-
P10	T0G	GPIO	ANA	MISO	SDA	-	C0_The	-	-
P11	-	GPIO	ANA	SCK	SCL	FB0	-	-	-
P12	T2EX	GPIO	ANA	NSS（SSO1）	-	FB1	-	-	-
P13	CUSTOM	GPIO	ANA	-	RXD	-	CLO	-	-
P14	CAPE 3	GPIO	ANA	-	TXD	PG3	CC3	-	-
P15	T1G/CAP2	GPIO	ANA	-	-	PG2	CC2	-	-
P16	T2	GPIO	ANA	-	-	PG1	-	-	-
P17	T2EX	GPIO	ANA	-	-	PG0	BUZZ	-	-
P20	-	GPIO	ANA	-	-	PG0	C1_The	-	-
P21	T1G	GPIO	ANA	-	RXD	PG1	-	-	-
P22	T0G	GPIO	ANA	-	TXD	PG2	-	-	-
P23	-	GPIO	ANA	-	-	PG3	BUZZ	-	-
P24	T1/NRST	GPIO	ANA	-	-	-	C1_O	-	-
P25	T0/NRST	GPIO	ANA	-	-	-	-	-	-
P30	INT0	GPIO	ANA	-	-	-	-	-	-
P31	INT1	GPIO	ANA	-	-	-	-	-	-
P32	-	GPIO	ANA	-	-	-	-	-	-
P33	-	GPIO	ANA	-	-	-	-	-	-

Analog Ports, CONFIG Configuration Ports List:

	ANA(1)				CONFIG
	ADC	LCDSEG	LCDCOM	ACMP	
P00	AN0	SEG0	COM0	C1P2	-
P01	AN1	-	-	-	-
P02	AN2	SEG21	COM21	-	-
P03	AN3	SEG22	COM22	-	-
P04	AN4	SEG1	COM1	-	-
P05	AN5	SEG23	COM23	-	-
P06	AN6	SEG2	COM2	C1P3	-
P07	AN7	-	-	-	-
P10	AN8	SEG3	COM3	-	-
P11	AN9	SEG4	COM4	C0P0	-
P12	AN10	SEG5	COM5	C0N	-
P13	AN11	SEG6	COM6	-	-
P14	AN12	SEG7	COM7	-	-
P15	AN13	SEG8	COM8	-	-
P16	AN14	SEG9	COM9	-	-
P17	AN15	SEG10	COM10	-	-
P20	AN16	SEG11	COM11	-	-
P21	AN17	SEG12	COM12	C1P0	-
P22	AN18	SEG13	COM13	C1N	-
P23	AN19	SEG14	COM14	C1P1	-
P24	AN20	SEG15	COM15	-	-
P25	AN21	SEG16	COM16	-	-
P30	AN22	SEG17	COM17	-	XTOUT
P31	AN23	SEG18	COM18	-	XTIN
P32	AN24	SEG19	COM19	-	OSCIN
P33	AN25	SEG20	COM20	-	OSCOUT

Note: 1. The chip pins are subject to the actual chip.

2. All pins support the COM SEG function of leDs.

4. Feature Summary

4.1 System Clock

The system clock has four clock sources, which can be selected by setting the system configuration register or user register. The system clock module has the following features:

- Internal high-speed oscillation HSI (48MHz).
- External high-speed crystal oscillation HSE (8MHz/16MHz).
- External low-speed crystal oscillation LSE (32.768KHz).
- Internal low-speed oscillation LSI (125KHz).
- Any two clock sources can be switched to each other.
- External high-speed and low-speed oscillators support the stop-oscillation monitoring function (SCM) when the system clock is provided.

4.2 Reset

The reset operation is used to initialize the internal circuitry of the chip, allowing the system to start working from a determined state. The chip has the following reset methods:

- Power-on reset.
- External reset.
- Low voltage reset.
- CONFIG status protection reset.
- Power-on configuration monitor reset.
- Watchdog overflow reset.
- Software reset.

Any of the above reset situations require a certain response time, and the system provides a perfect reset process to ensure the smooth progress of the reset operation.

4.3 Power Management

4.3.1 Working Mode

The chip has 3 different operating modes to adapt to the power consumption requirements of different applications.

- Normal operating mode: The MCU is in normal working condition and the peripherals are operating normally.
- Idle mode IDLE: The MCU is in idle mode, the CPU stops working, and the peripherals are running normally. This mode can be woken up by any interrupt.
- Hibernate mode STOP: The MCU is in sleep mode, the CPU stops working, and the peripherals stop working. This mode can be woken up by INT0/1 interrupt, external interrupt wake-up, WUT timed wake-up, LSE timed wake-up.

4.3.2 Power Supply Low Voltage Reset (LVR)

When the supply voltage falls below the set sense voltage, the system resets.

There are four options for low-voltage reset: 1.8V/2.0V/2.5V/3.5V.

4.3.3 Power Supply Low Voltage Detection (LVD)

The low voltage detection circuit compares the supply voltage to the set voltage and generates an interrupt request signal if the supply voltage is lower than the set voltage.

The programmable detection voltage range is 2.0V to 4.6V, and a total of 16 levels are available.

4.4 Interrupt Control

The chip has multiple interrupt sources and interrupt vectors, and the user-programmable interrupts include INT0/1, Timer0/1, Timer2, Timer3/4, WDT, LSE_Timer (SCM), PWM, I2C、SPI、UART0、P0/P1/P2/P3、ACMP0/1、 The actual number of ADCs, LVDs, and interrupt sources varies by product.

The chip specifies two interrupt priorities, allowing for two levels of interrupt nesting. When an interrupt has already responded, if a high-level interrupt is requested, the latter can interrupt the former, realizing interrupt nesting.

4.5 Timer

4.5.1 WDT Timer

The watchdog timer is an on-chip timer that is provided by the system clock and overflows with WDT timing will produce a reset. Watchdog reset is a protective setting of the system, when the system is running to an unknown state, the watchdog can be used to reset the system, thereby avoiding the system from entering an indefinite dead loop. WDT timers have the following features:

- Watchdog overflow time 8 levels optional.
- Watchdog overflow interrupt can be set.
- Watchdog overflow reset can be set.

4.5.2 Timer Counter 0/1 (Timer0/1)

Timer 0 is similar in type and structure to Timer 1 and is two 16-bit up counting timers. Timer0 has 4 modes of operation and Timer1 has 3 modes of operation, which provide basic timing and event counting operations.

In "timer mode", the timing register is incremented every 12 or 4 system cycles when the timer clock is enabled. In "counter mode", the timing register increments whenever it detects a falling edge on the corresponding input pin (T0 or T1). Timer0/1 has the following features:

- Can be used as a normal timer.
- Can be used for gated timer functions.
- External counting function can be implemented.
- Can be used for gated counting functions.
- The counter overflow interrupts.

4.5.3 Timer Counter 2 (Timer2)

Timer 2 is a 16-bit timer that can be used for the generation of various digital signals and event capture, such as pulse generation, pulse width modulation, pulse width measurement, etc. Timer2 has the following features:

- Can be used as a normal timer.
- Can be used for gated timer functions.
- External counting function can be implemented.
- It has the functions of reload prohibition, overflow automatic reload, and automatic reloading of external pin falling edge.
- Capture can be triggered by the rising edge, falling edge, double edge, or low byte of the write capture register.
- Features a comparison function that generates a periodic signal with a controllable duty cycle of the PWM waveform.
- Timing, external triggering, capture, and comparison can all produce interrupts.

4.5.4 Timer 3/4 (Timer3/4)

Timer 3/4 is similar to timer 0/1 in that it is two 16-bit timers. Timer3 has 4 working modes and Timer4 has 3 working modes. In contrast to Timer0/1, Timer3/4 only provides timer operations.

With the timer activated, the value of the register is incremented every 12 or 4 system cycles.

4.5.5 LSE Timer (LSE_Timer)

The LSE timer is a clock source from an external low-speed clock LSE, a 16-bit up-counting timer. LSE timers have the following features:

- Timer function.
- A 16-bit timer value can be set.
- Works in sleep mode.
- An interrupt can occur when the count value is equal to the timer value.
- A timed interrupt wakes up idle mode/sleep mode.

4.5.6 Wake-up Timer (WUT)

The WUT wake-up timer is a clock source from the internal low-speed clock LSI, a 12-bit, up-count timer for sleep wake-ups. After the system enters sleep mode, the CPU stops working with all peripheral circuitry, and the internal low-speed clock LSI provides a clock to the WUT counter. WUT has the following features:

- The system can be woken up at a configured time during sleep.
- The counting clock is available in divide-by-1, 8, 32, and 256.
- A 12-bit timer value can be set.
- The timing overflow status can be queried.

4.5.7 Baud Rate Timer (BRT)

The BRT timer is a 16-bit baud rate timer (its clock source is from the system clock), which mainly provides the clock for UART module. BRTs have the following features:

- Has an independent control switch.
- The counting clock has an 8-levels frequency division option.
- 16-bit increment count.

4.6 Enhanced Digital Peripherals

4.6.1 Buzzer Driver (BUZZER)

The buzzer drive module consists of an 8-bit counter, clock driver, control register, and a square wave with an output duty cycle of 50% and a frequency covering a wide range. BUZZER has the following features:

- Has a separate enable control switch.
- The clock division ratio of 8, 16, 32, and 64 can be set.
- The output frequency is 8-bit controllable, and the output can be set (1~255) x 2 frequency division.

4.6.2 Enhanced PWM Module

The Enhanced PWM Module supports 4-channel PWM generators with independently programmable cycles and duty cycles. PWM has the following features:

- Supports two kinds of waveform outputs in single-shot and continuous mode.
- Supports four control modes: independent, complementary, synchronous, and group control.
- The counting clocks are available in divide-by-1, 2, 4, 8, and 16.
- Two counting modes are supported, edge alignment and center alignment, and symmetric and asymmetric counting are supported in center alignment mode.
- Mask output is supported.
- Supports dead-zone programming.
- Output polarity can be set.
- Supports period, up-compare, down-compare, zero-point interrupt.
- Supports software brakes, external port trigger brakes, ADC comparison results trigger brakes, ACMP output trigger brakes, and four brake recovery modes.

4.7 Display Interface

4.7.1 LCD Driver

Supports software-driven COM and SEG outputs. This hardware circuit has the following characteristics:

- Up to 24 COM ports, 24 SEG ports are supported.
- 1/3BIAS.

4.7.2 LED Driver

Support software LED display driver. This hardware circuit has the following characteristics:

- Up to 24 COM ports, 24 SEG ports are supported.
- COM port current two gears are optional.
- SEG port current 4 gears optional.

4.8 Communication Module

4.8.1 SPI Module

The SPI is a fully configurable SPI master/slave device that allows the user to configure the polarity and phase of the serial clock signal. SPI allows the MCU to communicate with serial peripherals, and it is also capable of interprocessor-to-processor communication in multi-host systems. SPI has the following features:

- Full-duplex synchronous serial data transfer.
- Supports master/slave mode.
- Support for multi-host systems.
- System error detection.
- Supports speeds up to 1/4 of the system clock (F_{SYS}≤24MHz).
- The bit rate produces 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 of the system clock.
- Four transmission formats are supported.
- Send/receive completion can produce an interrupt.

4.8.2 I²C Module

The two-wire bidirectional serial bus controller I2C provides a simple and efficient connection for data exchange between the microprocessor and the I2C bus. The I2C module has the following features:

- Support 4 working modes: master transmission, master reception, slave transmission, slave reception.
- Supports 2 transfer speed modes:
  Standard (up to 100Kb/s);
  Fast (up to 400Kb/s).
- Perform arbitration and clock synchronization.
- Support for multi-host systems.
- The host mode supports7-bit addressing mode and 10-bit addressing mode on the I2C-bus (software supported).
- Slave mode supports7-bit addressing mode on the I2C-bus.
- Allows operation over a wide clock frequency range (built-in 8-bit timer).
- Receive/send completion can produce an interrupt.

4.8.3 UART0 Module

UART0 has the following features:

- Full-duplex serial port.
- Synchronous mode is supported.
- Supports 8-bit asynchronous transceiver mode with variable baud rate.
- Supports a 9-bit asynchronous transceiver mode with variable baud rate
- Baud rates can be generated by timer1/Timer4/Timer2/BRT modules.
- Send/receive completion can produce an interrupt.

4.9 Analog Module

4.9.1 Analog-to-digital Converter (ADC).

The ADC module is a 12-bit successive approximation analog-to-digital converter. The port analog input signal is connected to the input of the analog-to-digital converter after passing through a multiplexer, which generates a 12-bit binary result based on the input analog signal and saves the result in the ADC result register. ADCs have the following characteristics:

- Up to 26 external channels.
- The conversion clock of the ADC is available in eight clock frequencies.
- The ADC reference voltage can be selected from VDD/1.2V/2.0V/2.4V/3.0V.
- A full 12-bit conversion requires 18.5 ADC conversion cycles.
- Supports external port edges, enhanced PWM trigger ADC conversion.
- Support ADC conversion result comparison output, comparison output can control the enhanced PWM brake function.
- Supports interrupt generation when an ADC conversion is complete.

4.9.2 Analog Comparator (ACMP0/1)

The comparators ACMP0 and ACMP1 have the following features:

- The positive side supports multiple input ports to select.
- The negative side can select the port input or internal reference voltage.
- Internal reference divider step is selectable.
- Support output filtering, filtering time step can be selected.
- Supports unilateral and bilateral hysteresis control.
- Hysteresis voltage seletion is available at 10/20/60mV.
- Supports software trimming of offset voltage.
- The output acts as a brake trigger signal for the enhanced PWM.
- Supports output changes to produce interrupts.

4.9.3 Temperature Sensor (TS)

This series consists of 1 temperature sensor with the following characteristics:

- Measurable temperature range: -40°C~105°C.
- Software trimming is possible.
- The output can be measured by an ADC.

4.10 FLASH memory

FLASH memory contains program memory (APROM/BOOT) and non-volatile data memory (Data FLASH), which can be correlated by passing Special Function Registers (SFR) access it to implement IAP functionality. Flash memory supports the following operations:

- Byte read operation.
- Byte write operations.
- Page erase operation.
- FLASH space CRC check operation.

4.11 Unique ID (UID)

Each chip has a 96-bit unique identification number, known as Unique identification. The UID is already set at the factory and cannot be modified by the user.

5. User Configuration

The System Configuration Register (CONFIG) is a FLASH option for the initial conditions of the MCU and cannot be accessed or operated by the program. The system configuration register allows you to set the following:

- The way watchdogs work.
- FLASH program area partition protection, code encryption, FLASH data area encryption status.
- Charged flash function.
- Low voltage reset voltage.
- Debug mode disable or enable.
- Oscillation mode, prescale selection.
- Internal high-speed oscillator frequency division selection.
- External reset configuration, port selection.
- Sleep wake-up wait time.
- APROM/BOOT space.

6. Electrical Parameters

Unless otherwise specified, the temperature condition TA=25℃ for the following parameters.

6.1 Absolute Maximum Rating

symbol	parameter	minimum	maximum	unit
T_{ST}	Storage temperature	-55	150	℃
T_A	Operating temperature	-40	105	℃
VDD-VSS	Supply voltage	-0.3	5.8	V
IN_{AND}	Input voltage	VSS-0.3	VDD+0.3	V
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	200	mA
THE_{IOs}	Maximum sink current for a single IO	-	50	mA
	Maximum Sink Current for a Single IO (LED COM)	-	150	mA
	Maximum current for a single IO	-	45	mA
	Single IO Maximum Current Pull (LED SEG)	-	45	mA
	Maximum sink current for all IO	-	200	mA
	Maximum pull current for all IO	-	120	mA

Note: If the operating conditions of the device exceed the range of "**absolute maximum rating**", the device will be permanently damaged. Only when the device works within the scope specified in the manual can the function be guaranteed. If the chip is at the absolute maximum rating, the reliability of the device may be affected.

6.2 DC Electrical Characteristics

VDD-VSS=2.1～5.5V，T_A=25℃

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
VDD	Operating voltage	F_{SYS}=48MHz，F_{CPU}=F_{SYS}/2 F_{SYS}=8MHz~24MHz，F_{CPU}=F_{SYS}	2.1	-	5.5	V
I_{DD}	Normal mode	VDD=5V, F_{SYS}=48MHz, all peripherals off F_{CPU}=F_{SYS}/2	-	6.5	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off F_{CPU}=F_{SYS}/2	-	6.5	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are off F_{CPU}=F_{SYS}	-	4.5	-	mA
		VDD=3V, F_{SYS}=24MHz, all peripherals are off F_{CPU}=F_{SYS}	-	4.5	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off F_{CPU}=F_{SYS}	-	3.5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off F_{CPU}=F_{SYS}	-	3.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off F_{CPU}=F_{SYS}	-	2.5	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off F_{CPU}=F_{SYS}	-	2.5	-	mA
	IDLE mode	VDD=5V, F_{SYS}=48MHz, all peripherals off	-	5	-	mA
		VDD=3V, F_{SYS}=48MHz, all peripherals off	-	5	-	mA
		VDD=5V, F_{SYS}=24MHz, all peripherals are	-	3	-	mA

		off				
		VDD=3V, F_{SYS}=24MHz, all peripherals are off	-	3	-	mA
		VDD=5V, F_{SYS}=16MHz, all peripherals are off	-	2.5	-	mA
		VDD=3V, F_{SYS}=16MHz, all peripherals are off	-	2.5	-	mA
		VDD=5V, F_{SYS}=8MHz, all peripherals off	-	2	-	mA
		VDD=3V, F_{SYS}=8MHz, all peripherals are off	-	2	-	mA
I_{SLEEP1}	Sleep current	VDD=3V, all peripherals are off and LSE, LSE timers are enabled	-	20	-	uA
I_{SLEEP2}	Sleep current	VDD=3V, all peripherals are off and LSI, WUT timers are enabled	-	7	-	uA
I_{SLEEP3}	Sleep current	VDD=3V, all peripherals are turned off	-	6	-	uA
I_{LI}	Input leakage	-	-1	-	1	uA
V_{IL}	Enter a low level	-	VSS	-	0.3VDD	V
V_{IH}	Enter high	-	0.7VDD	-	VDD	V
V_{OL}	Output low voltage	VDD=5V,I_{OL1}=18mA	-	-	0.4	V
		VDD=5V，I_{OL2}=50mA（LED COM）	-	-	0.4	V
		VDD=3V,I_{OL1}=12mA	-	-	0.4	V
		VDD=3V，I_{OL2}=22mA（LED COM）	-	-	0.4	V
V_{OH}	Output high voltage	VDD=5V,I_{OH1}=45mA	3.5	-	-	V
		VDD=5V,I_{OH2}=45mA（LED SEG Max）	3.5	-	-	V
		VDD=5V,I_{OH3}=3mA (LED HIMSELF Min)	3.5	-	-	V
		VDD=3V,I_{OH1}=18mA	2.1	-	-	V
		VDD=3V,I_{OH2}=18mA（LED SEG Max）	2.1	-	-	V
		VDD=3V,I_{OH3}=1mA(LED MIN)	2.1	-	-	V
R_{PH}	Pull-up resistor	-	-	32	-	KΩ
R_{PL}	Pull-down resistor	-	-	32	-	KΩ

6.3 AC Electrical Parameters

6.3.1 Power-up and Power-down Operation

T_A= 25°C, excluding 32.768K crystal resonant time

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
T_{RESET}	Reset time	VDD=5V	-	16	-	ms
TVDDR	VDD rise rate	VDD=5V	20	-	-	us/V
TVDDF	VDD fall rate	VDD=5V	20	-	-	us/V

6.3.2 External Oscillator

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_{HSE}	Operating voltage	F=8/16MHz, C_{XT}=0-47pF	2.1	-	5.5	V
V_{LSE}	Operating voltage	F=32.768KHz, C_{XT}=10-22pF	2.1	-	5.5	V

6.3.3 Internal Oscillator

VDD=2.1V-5.5V

symbol	parameter	Test conditions	Frequency error	minimum	Typical	maximum	unit
F_{HSI}	Internal high speed 48MHz	T_A=25℃	±1%	-	48	-	MHz
		T_A=-20℃ to 85℃	±2%	-	48	-	MHz
		T_A=-40℃ to 105℃	±3%	-	48	-	MHz
F_{LSI}	Internal low speed 125KHz	T_A=25℃	±10%	-	125	-	KHz
		T_A=-40℃ to 105℃	±15%	-	125	-	KHz

6.3.4 Low-voltage Reset Electrical Parameters

symbol	parameter	minimum	Typical	maximum	unit
V_{LVR1}	Low pressure detection threshold 1.8V	1.65	1.8	1.95	V
V_{LVR2}	Low pressure detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVR3}	Low pressure detection threshold 2.5V	2.35	2.5	2.65	V
V_{LVR4}	Low pressure detection threshold 3.5V	3.35	3.5	3.65	V

6.3.5 LVD Electrical Parameters

symbol	parameter	minimum	Typical	maximum	unit
V_{LVD1}	Low pressure detection threshold 2.00V	1.90	2.00	2.10	V
V_{LVD2}	Low pressure detection threshold 2.16V	2.06	2.16	2.26	V
V_{LVD3}	Low pressure detection threshold 2.31V	2.21	2.31	2.41	V
V_{LVD4}	Low pressure detection threshold 2.45V	2.35	2.45	2.55	V
V_{LVD5}	Low pressure detection threshold 2.60V	2.50	2.60	2.70	V
V_{LVD6}	Low pressure detection threshold 2.73V	2.63	2.73	2.83	V
V_{LVD7}	Low pressure detection threshold 2.88V	2.78	2.88	2.98	V
V_{LVD8}	Low pressure detection threshold 2.98V	2.88	2.98	3.08	V
V_{LVD9}	Low pressure detection threshold 3.21V	3.11	3.21	3.31	V
V_{LVD10}	Low pressure detection threshold 3.42V	3.32	3.42	3.52	V
V_{LVD11}	Low pressure detection threshold 3.62V	3.52	3.62	3.72	V
V_{LVD12}	Low pressure detection threshold 3.81V	3.71	3.81	3.91	V
V_{LVD13}	Low pressure detection threshold 4.00V	3.90	4.00	4.10	V
V_{LVD14}	Low pressure detection threshold 4.20V	4.10	4.20	4.30	V
V_{LVD15}	Low pressure detection threshold 4.43V	4.33	4.43	4.53	V
V_{LVD16}	Low pressure detection threshold 4.60V	4.50	4.60	4.70	V

6.4 FLASH Electrical Parameters

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_F	FLASH operating voltage	-	2.1	-	5.5	V
T_F	FLASH operating temperature	-	-40	25	105	℃
$N_{ENDURANCE}$	The number of erases and writes	Program FLASH	20,000	-	-	Cycle
		Data FLASH	100,000	-	-	
T_{RET}	Data retention time	25℃	100	-	-	year
T_{ERASE}	Sector erase time	-	-	1.5	-	ms
T_{WRITE}	Write time			30		us
T_{READ}	Reading time	-	-	3*Tsys	-	-
I_{DD1}	Read current	-	-	-	2.5	mA
I_{DD2}	Programming current	-	-	-	3.6	mA
I_{DD3}	Erase current	-	-	-	2	mA

6.5 Simulation Characteristics

6.5.1 BANDGAP Electrical Characteristics

T_A=25℃

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
V_{BG}	Internal reference 1.2V	VDD=2.1~5.5V、T_A=25℃	1.188	1.2	1.212	V
		VDD=2.1~5.5V、T_A=-20℃至 85℃	1.182	1.2	1.218	V
		VDD=2.1~5.5V、T_A=-40℃至 105℃	1.176	1.2	1.224	V

6.5.2 ADC Electrical Characteristics

T_A=25℃

symbol	parameter		minimum	Typical	maximum	unit
V_{AVDD}	ADC operating voltage		2.5	-	5.5	V
V_{REF1}	Reference voltage 1		-	IN_{AVDD}	-	V
V_{REF2}	Reference voltage 2 (non-V_{BG}).		1.185	1.2	1.215	V
V_{REF3}	Reference voltage 3		1.985	2.0	2.015	V
V_{REF4}	Reference voltage 4		2.385	2.4	2.415	V
V_{REF5}	Reference voltage 5		2.985	3.0	3.015	V
V_{ADI}	Input voltage		0	-	V_{REF}	V
N_R	resolution		12			Bit
DNL	Differential nonlinearity error (V_{REF}=V_{AVDD}=5V, T_{ADCK}=0.5us).		±2			LSB
INL	Integral nonlinearity error (V_{REF} =V_{AVDD}=5V, T_{ADCK}=0.5us).		±4			LSB
T_{ADCK}	ADC clock cycle	V_{REF}=VDD=5V	0.5	-	-	us
		V_{REF}=V_{REF2}	32	-	-	us
		V_{REF}=V_{REF3}/ V_{REF4}/V_{REF5}	2	-	-	us
I_{ADC}	ADC conversion time		-	18.5	-	T_{ADCK}
F_S	sample rate(V_{REF}=V_{AVDD}=5V)		100			Ksps

Note: When V_{REF}=V_{REF2}, the precision is 8bit.

6.5.3 ACMP Electrical Characteristics

T_A=25°C, V_{SENSE}=V_{IN+}-V_{IN-}, VDD=5V, V_{IN+}=1V, unless specified otherwise

symbol	parameter	condition	minimum	Typical	maximum	unit
VDD	Supply voltage	-	2.1	-	5.5	V
I_Q	Quiescent current	V_{SENSE}=0.1V	-	0.2	0.3	mA
I_{SD}	Shut down the current	V_{SENSE}=0.1V	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input properties						
V_{OS}	Input offset voltage	Unmodified (C0CON1 [4:0] = 10H).	-	±4.0	-	mV
		After zeroing	-	±0.5	±1.0	
V_{CM}	Common-mode input voltage range	-40℃~105℃	-0.1	-	VDD-1. 3	V
I_B	Input bias current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output properties						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristics						
A_{OL}	Open-loop gain	-	-	90	-	dB
BW	bandwidth	-	-	200	-	MHz
PSRR	Power supply rejection ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common mode rejection ratio	VDD=2.1~5.5V -40℃~105℃	-	100	-	dB
Transient characteristics						
T_{STB}	Settling time	-	-	-	5	us
T_{PGD}	Response delay	In_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

6.5.4 Temperature Sensor Electrical Characteristics

VDD-5V

symbol	parameter	Test conditions	minimum	Typical	maximum	unit
T_{LINE}	Linearity	-	-	±4	-	℃
K_{AVG}	slope	-40℃~105℃	3.3	3.5	3.7	mV/°C
V_{25}	25°C output voltage	T_A=25℃	0.99	1	1.01	V
T_S	Establishment time	-	-	-	10	us
T_{SMP}	The sampling time of the ADC	-	150	-	-	us

Note: Design guarantee.

6.6 EMC Features

6.6.1 EFT Electrical Characteristics

symbol	parameter	Test conditions	maximum	unit	grade
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDDand VSSpins to induce a functional disturbance	T_A= + 25℃, F_{SYS}=48MHz, conforms to IEC 61000-4-4	4800	V	4B

Note: The immunity performance of electrical fast transient pulse swarm (EFT) is closely related to the system design (including power supply structure, circuit design, layout and wiring, chip configuration, program structure, etc.). The EFT parameters in the table above are measured on the CMS internal test platform and are not suitable for all application environments, and the test data is for reference only. All aspects of the system design may affect the EFT performance, in the application of high EFT performance requirements, the design should pay attention to avoid interference sources affecting the operation of the system, it is recommended to analyze the interference path and optimize the design to achieve the best immunity performance.

6.6.2 ESD Electrical Characteristics

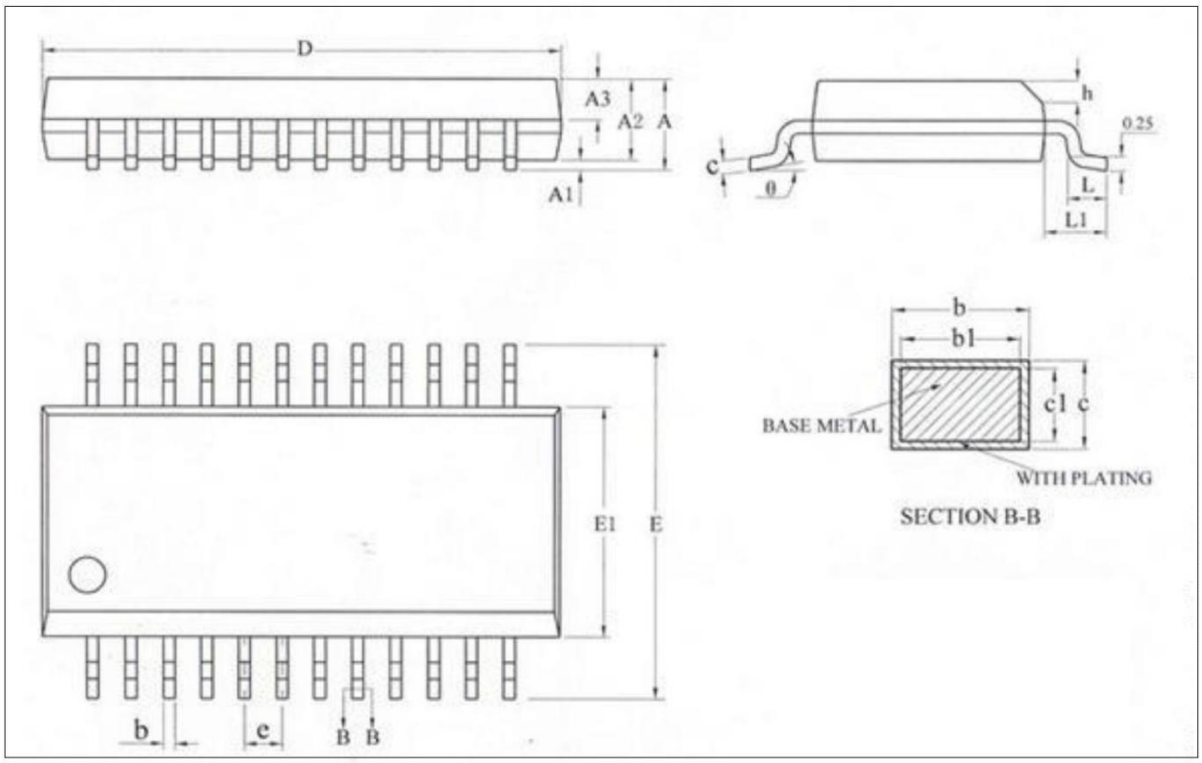
symbol	parameter	Test conditions	maximum	unit	grade
V_{ESD}	Electrostatic discharge (Human discharge mode HBM)	T_A= + 25℃, JEDEC EIA/JESD22- A114	8000	V	3B
	Electrostatic discharge (Machine discharge mode MM)	T_A= + 25℃, JEDEC EIA/JESD22- A115	400	V	C

6.6.3 Latch-Up Electrical Characteristics

symbol	parameter	Test conditions	The test type	minimum	unit
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (T_A = +25℃)	±200	mA

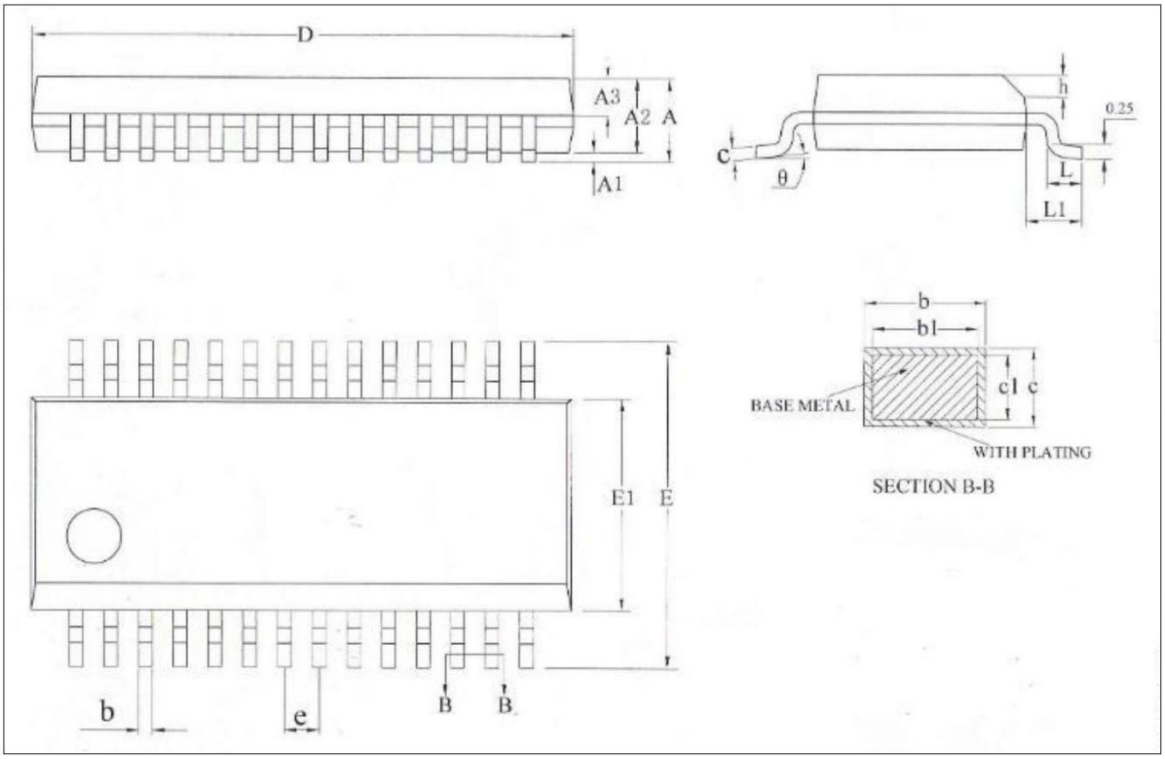
7. Packaging Information

7.1 SSOP24



Symbol	Millimetre		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

7.2 SSOP28



Symbol	Millimetre		
	Min	Nom	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

8. Version History

The version number	Time	Revision content
V1.00	October 2019	Initial release
V1.01	February 2020	Modify the information corresponding to the INT pin
V1.02	January 2023	Correct FLASH electrical parameters
V1.03	January 2023	1) 6.1 Absolute Maximum Rating: Notes on limit parameters added 2) Modify 6.2 DC Electrical Characteristics 3) 6.3.1 Power-up and Power-down Operation: adjust parameters 4) 6.3.3 Internal Oscillator: adjust parameters 5) 6.4 FLASH Electrical Parameters: Description of optimizing write and read times 6) 6.5.1 BANDGAP Electrical Characteristics: Refine parameters 7) 6.5.2 ADC Electrical Characteristics: ADC clock cycle is described according to different reference voltages 8) 6.5.3 ACMP Electrical Characteristics: Optimize parameters, add comments 9) 6.5.4 Temperature Sensor Electrical Characteristics: Optimize parameters, add comments 10) 1.1 Features, 1.2 Product Comparison, 4.7.2 LED Driver, 2.1 System Introduction: Change COM/SEG quantity 11) Correction and unified text expression
V1.04	January 2023	Correct incorrect contents