SNx5LBC184 Differential Transceiver With Transient Voltage Suppression

1 Features

- Integrated transient voltage suppression
- ESD Protection for bus terminals exceeds:
  ±30kV IEC 61000-4-2, contact discharge
  ±30kV IEC 61000-4-2, Air-gap discharge
  ±15kV EIA/JEDEC Human body model
- Circuit damage protection of 400W peak (typical) per IEC 61000-4-5
- Controlled driver output-voltage slew rates allow longer cable stub lengths
- 250kbps in Electrically noisy environments
- Open-circuit fail-safe receiver design
- 1/4 Unit load allows for 128 devices connected on bus
- Thermal shutdown protection
- Power-up and power-down glitch protection
- Each transceiver meets or exceeds the requirements of TIA/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) standards
- Low disabled supply current 300µA maximum
- Pin compatible with SN75176

2 Applications

- Industrial networks
- Utility meters
- Motor control

3 Description

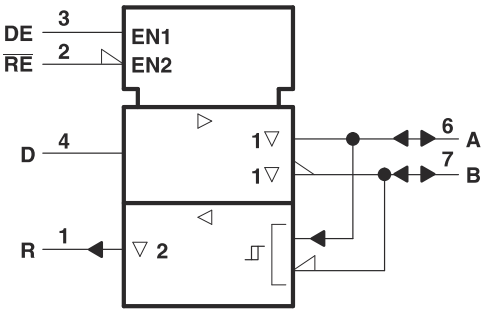
The SN75LBC184 and SN65LBC184 devices are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

The SN75LBC184 and SN65LBC184 can withstand overvoltage transients of 400W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN65LBC184, SN75LBC184	SOIC (8)	4.9mm × 6mm
	PDIP (8)	9.81mm × 6.35mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Symbol[1]

[1] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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4 Pin Configuration and Functions

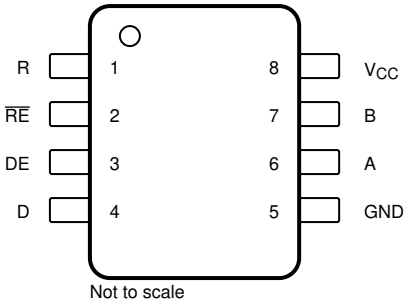


**Figure 4-1. D Package (SOIC), P Package (PDIP)
(Top View)**

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-HIGH driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receiver data output
$\overline{RE}$	2	Digital input	Active-LOW receiver enable
V_{CC}	8	Supply	4.75V to 5.25V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	7	V
	Continuous voltage range at any bus terminal	–15	15	V
	Data input/output voltage	–0.3	7	V
I_O	Receiver output current	–20	20	mA
	Continuous total power dissipation(3)	Internally Limited		
T_{stg}	Storage temperature		160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
(3) The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the *Section 5.9*.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, GND	±15000	V
			All pins	±3000	
		Contact discharge (IEC61000-4-2)(2)	A, B, GND(3)	±30000	
		Air discharge (IEC61000-4-2)	A, B, GND(3)	±30000	
		All pins (Class 3A)		±8000	
		All pins (Class 3B)		±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) GND and bus pin ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN(1)	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
$\lvert V_{ID}\rvert$	Differential input voltage				12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			4	
T_A	Operating free-air temperature	SN75LBC184	0		70	°C
		SN65LBC184	–40		85	

(1) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

5.4 Thermal Information

THERMAL METRIC[1]		P (PDIP)	D (SOIC)	UNIT
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.7	116.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.8	41.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	61.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.5	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOLS	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	NA	DE = $\overline{RE}$ = 5V	No Load		12	25	mA
			DE = 0 V, $\overline{RE}$ = 5V	No Load		175	300	µA
I_{IH}	High-level input current (D, DE, $\overline{RE}$)	NA	V_I = 2.4V				50	µA
I_{IL}	Low-level input current (D, DE, $\overline{RE}$)	NA	V_I = 0.4V		–50			µA
I_{OS}	Short-circuit output current OS(2)	NA	V_O = –7V		–250	–120		mA
			V_O = V_{CC}				250	
			V_O = 12V				250	
I_{OZ}	High-impedance output current	NA	See Receiver I_I					mA
V_O	Output voltage	V_{oa}, V_{ob}	I_O = 0		0		V_{CC}	V
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions	NA	See Figure 6-4 and Figure 6-5			0.8		V
V_{OC}	Common-mode output voltage	$\lvert V_{os}\rvert$	See Figure 6-3		1		3	V
$\lvert\Delta V_{OC(SS)}\rvert$	Magnitude of change, common-mode steady-state output voltage	$\lvert V_{os} - V_{os}\rvert$	See Figure 6-5				0.1	V
$\lvert V_{OD}\rvert$	Magnitude of differential output voltage $\lvert V_A - V_B\rvert$	V_o	I_O = 0		1.5		6	V
			R_L = 54Ω, See Figure 6-3		1.5			V
$\Delta\lvert V_{OD}\rvert$	Change in differential voltage magnitude between logic states	$\lvert\lvert V_t\rvert - \lvert V_t\rvert\rvert$	R_L = 54Ω				0.1	V

(1) All typical values are measured with T_A = 25°C and V_{CC} = 5V.
(2) This parameter is measured with only one output being driven at a time.

5.6 Electrical Characteristics: Receiver

over recommended operation conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current (total package)	DE = $\overline{RE}$ = 0 V, No Load				3.9	mA
		$\overline{RE}$ = 5V, DE = 0 V, No Load				300	µA
I_I	Input current	Other input = 0 V	V_I = 12V			250	µA
			V_I = 12V, V_{CC} = 0			250	
			V_I = –7V	–200			
			V_I = –7V, V_{CC} = 0	–200			
I_{OZ}	High-impedance-state output current	V_O = 0.4V to 2.4V				±100	µA
V_{hys}	Input hysteresis voltage				70		mV
V_{IT+}	Positive-going input threshold voltage					200	mV
$V_{IT–}$	Negative-going input threshold voltage			–200			mV
V_{OH}	High-level output voltage	I_{OH} = –8mA, See Figure 6-6		2.8			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA, See Figure 6-6				0.4	V

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

5.7 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(DH)}$	Differential output delay time, low-to-high-level output	R_L = 54Ω, C_L = 50pF	See Figure 6-4			1.3	µs
$t_{d(DL)}$	Differential output delay time, high-to-low-level output					1.3	µs
t_{PLH}	Propagation delay time, low-to-high-level output				0.5	1.3	µs
t_{PHL}	Propagation delay time, high-to-low-level output				0.5	1.3	µs
$t_{sk(p)}$	Pulse skew (| $t_{d(DH)} - t_{d(DL)}$|)				75	150	ns
t_r	Rise time, single-ended			0.25		1.2	µs
t_f	Fall time, single-ended			0.25		1.2	µs
t_{PZH}	Output enable time to high level	R_L = 110Ω	See Figure 6-1			3.5	µs
t_{PZL}	Output enable time to low level	R_L = 110Ω	See Figure 6-2			3.5	µs
t_{PHZ}	Output disable time from high level	R_L = 110Ω	See Figure 6-1			2	µs
t_{PLZ}	Output disable time from low level	R_L = 110Ω	See Figure 6-2			2	µs

5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Figure 6-6			150	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	ns
$t_{sk(p)}$	Pulse skew (|t_{PHL}– t_{PLH}|)				50	ns
t_r	Rise time, single-ended	See Figure 6-6		20		ns
t_f	Fall time, single-ended			20		ns
t_{PZH}	Output enable time to high level	See Figure 6-7			100	ns
t_{PZL}	Output enable time to low level				100	ns
t_{PHZ}	Output disable time from high level				100	ns
t_{PLZ}	Output disable time from low level				100	ns

5.9 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

5.10 Typical Characteristics

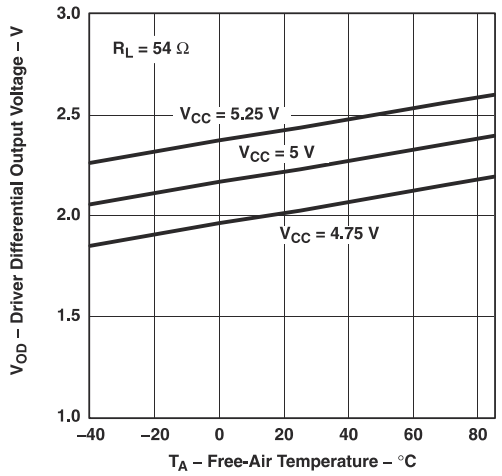


Figure 5-1. Driver Differential Output Voltage vs Free-Air Temperature

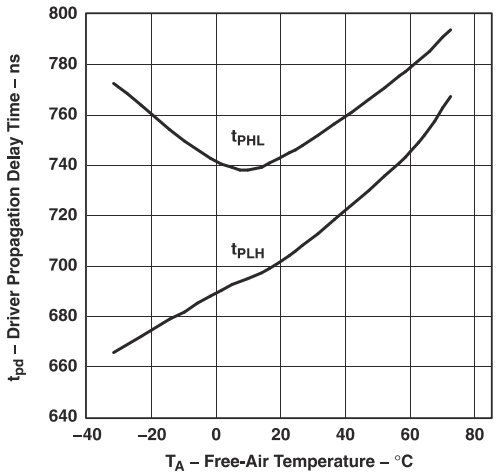


Figure 5-2. Driver Propagation Delay Time vs Free-Air Temperature

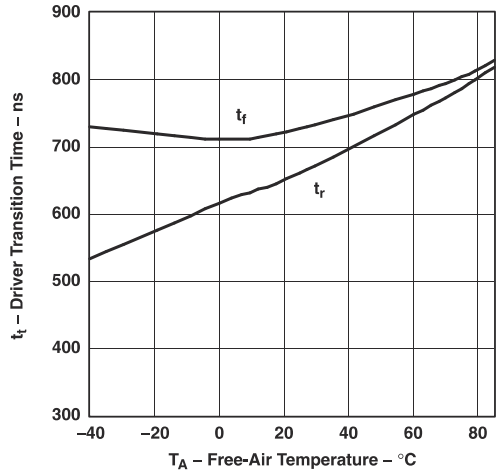


Figure 5-3. Driver Transition Time vs Free-Air Temperature

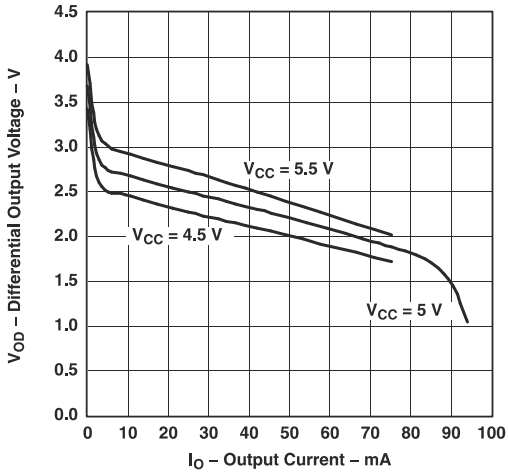


Figure 5-4. Differential Output Voltage vs Output Current

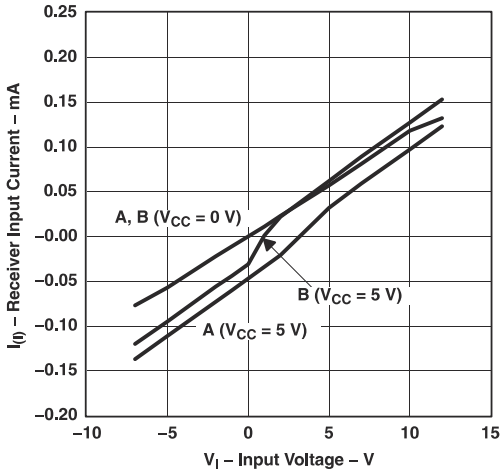
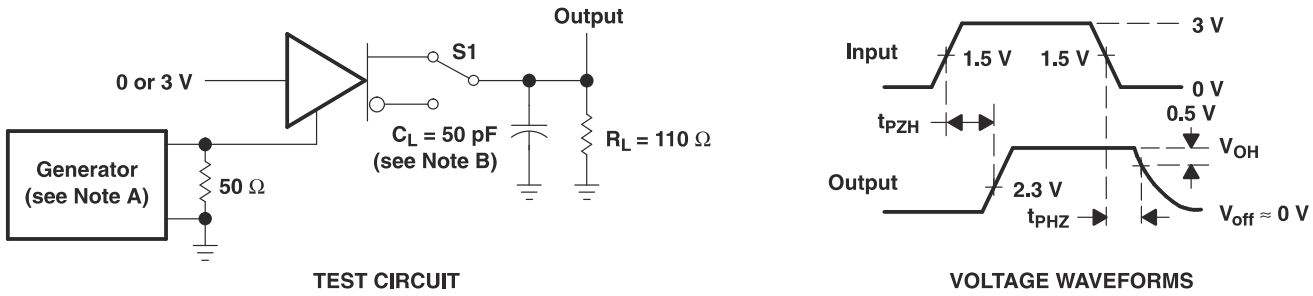


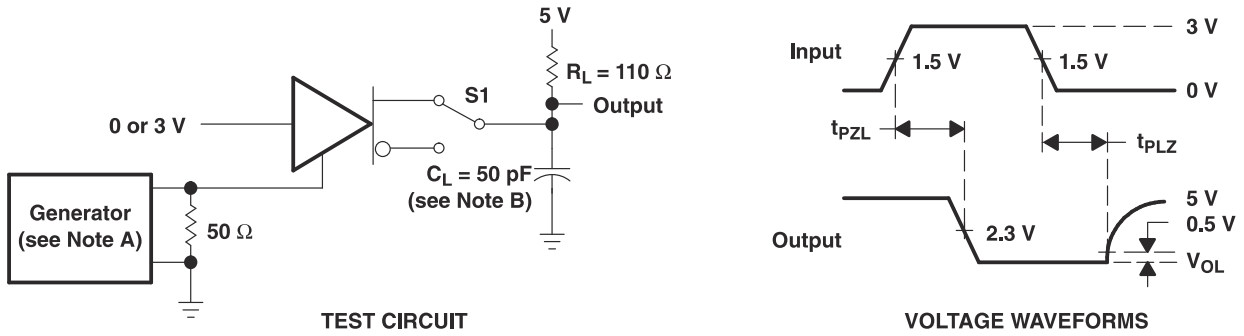
Figure 5-5. Receiver Input Current vs Input Voltage

6 Parameter Measurement Information



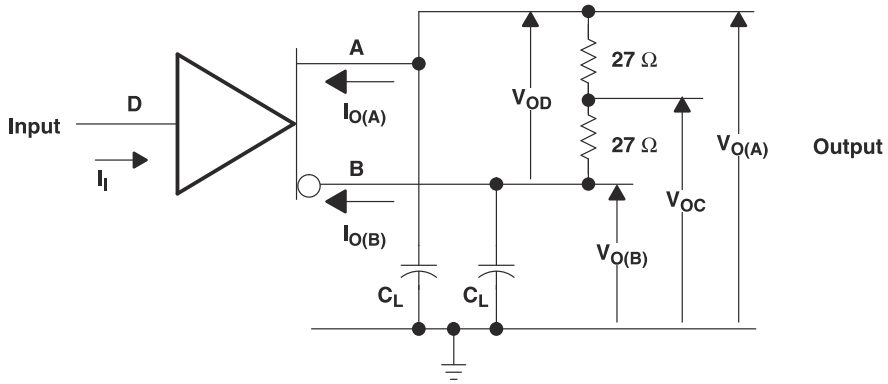
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6-1. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6-2. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



A. Resistance values are in ohms and are 1% tolerance.
B. C_L includes probe and jig capacitance.

Figure 6-3. Driver Test Circuit, Voltage, and Current Definitions

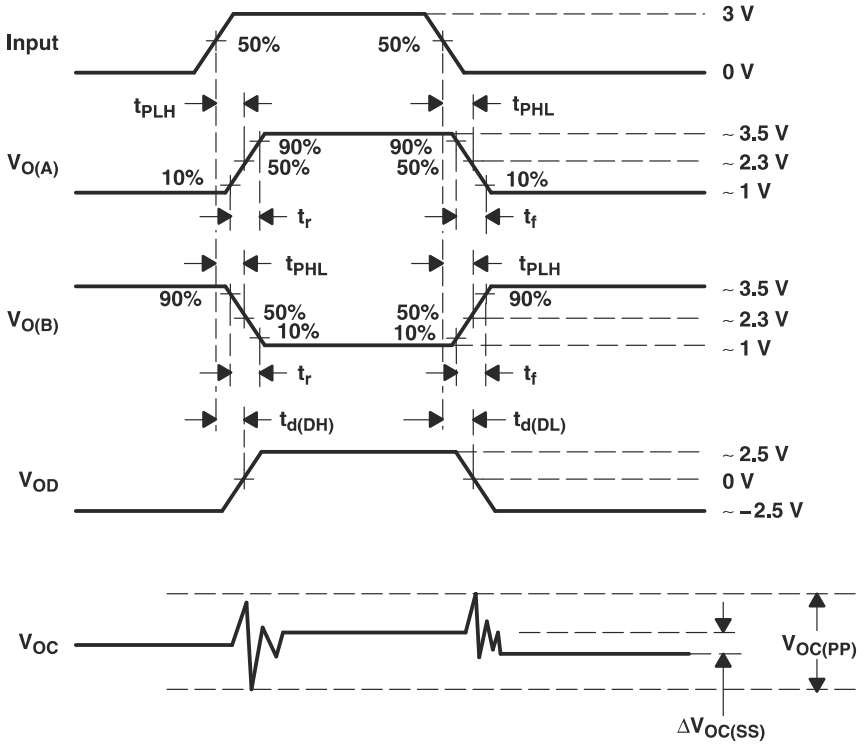
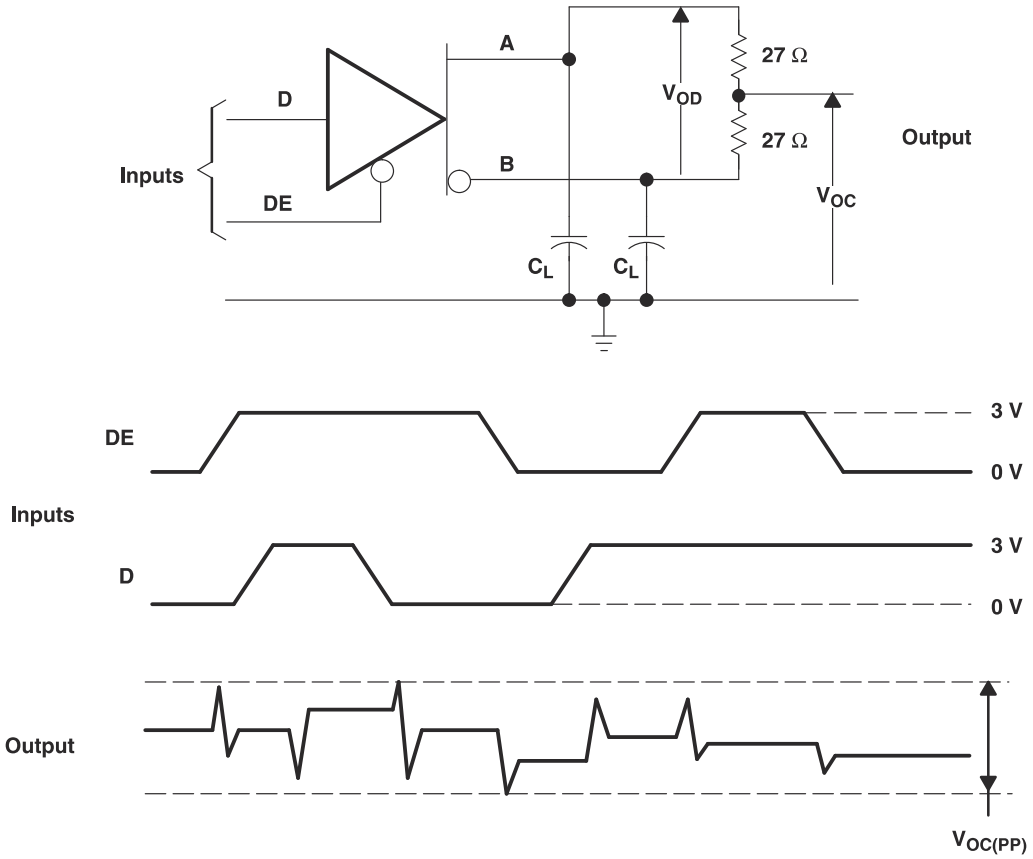


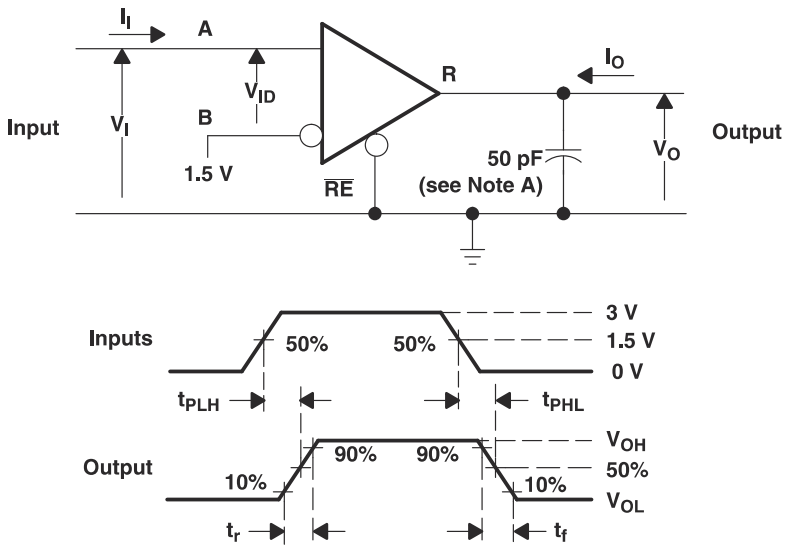
Figure 6-4. Driver Timing, Voltage, and Current Waveforms



A. Resistance values are in ohms and are 1% tolerance.

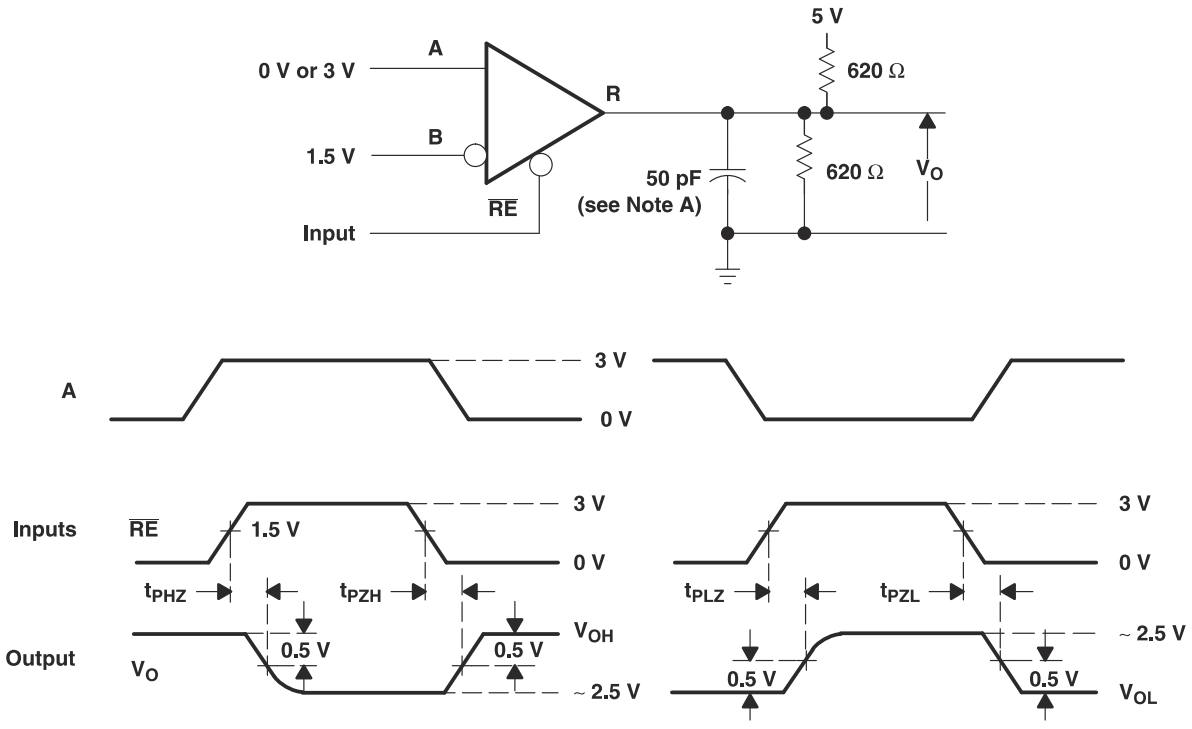
B. C_L includes probe and jig capacitance (±10%).

Figure 6-5. Driver $V_{OC(PP)}$ Test Circuit and Waveforms



A. This value includes probe and jig capacitance (±10%).

Figure 6-6. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



A. This value includes probe and jig capacitance (±10%).

Figure 6-7. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx5LBC184 device is a 5V, half-duplex, RS-485 transceiver with integrated transient voltage suppressors that prevent circuit damage in the presence of high-energy transients of up to 400W peak power. This transceiver has an active-HIGH driver enable and active-LOW receiver enable. The differential driver is suitable for data transmission up to 250kbps.

7.2 Functional Block Diagram

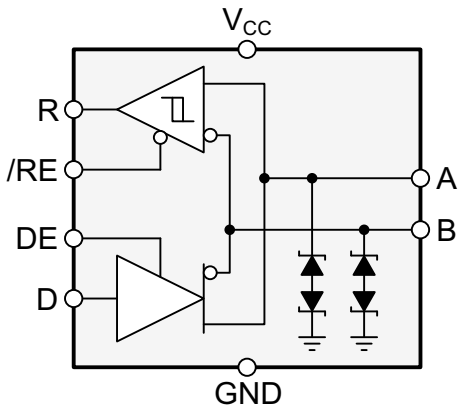


Figure 7-1. Functional Logic Diagram

7.3 Feature Description

Integrated transient voltage suppressors protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ±30kV and surge transients according to IEC 61000-4-5 of up to 400W peak.

The differential driver incorporates slew-rate controlled outputs sufficient to transmit data up to 250kbps. Slew-rate control allows for longer unterminated cable runs and longer stub lengths from the main cable trunk than with faster voltage transitions. A unique receiver design provides a high level failsafe output when the inputs are left floating.

The SN65LBC184 is characterized from –40°C to 85°C and the SN75LBC184 is characterized from 0°C to 70°C.

7.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant.

Table 7-1. Driver Functions

INPUT(1)	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$, the output is indeterminate.

When $\overline{RE}$ is logic high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. When the transceiver is disconnected from the bus, the receiver provides a failsafe high output.

Table 7-2. Receiver Functions

DIFFERENTIAL INPUT	ENABLE(1)	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT–} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT–}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
OPEN	L	H	Receiver failsafe High

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

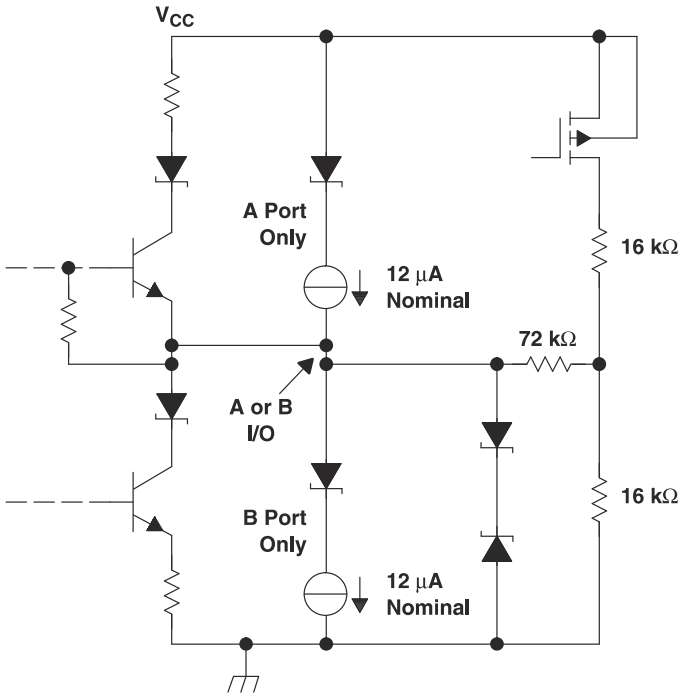


Figure 7-2. Schematic of Inputs and Outputs

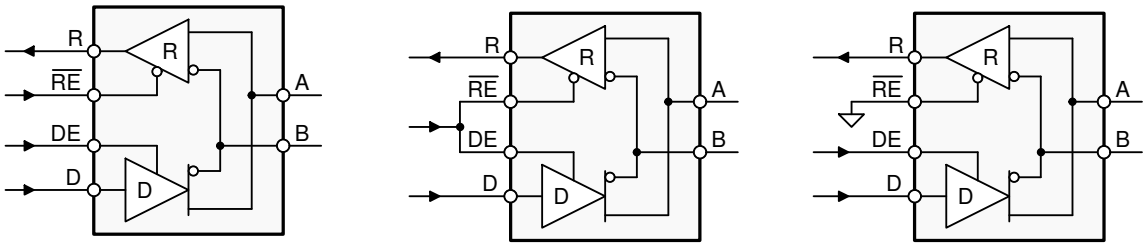
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN65LBC184 and SN75LBC184 devices are half-duplex, RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.



a) Independent driver and receiver enable signals

b) Combined enable signals for use as directional control pin

c) Receiver always on

Figure 8-1. Half-Duplex Transceiver Configurations

1. Using independent enable lines provides the most flexible control by allowing the driver and the receiver to be turned on and off individually. This configuration requires two control lines, allowing the selective listening into the bus traffic, whether the driver is transmitting data or not.
2. Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.
3. Only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also sends and verifies the correct data has been transmitted.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over a longer cable length.

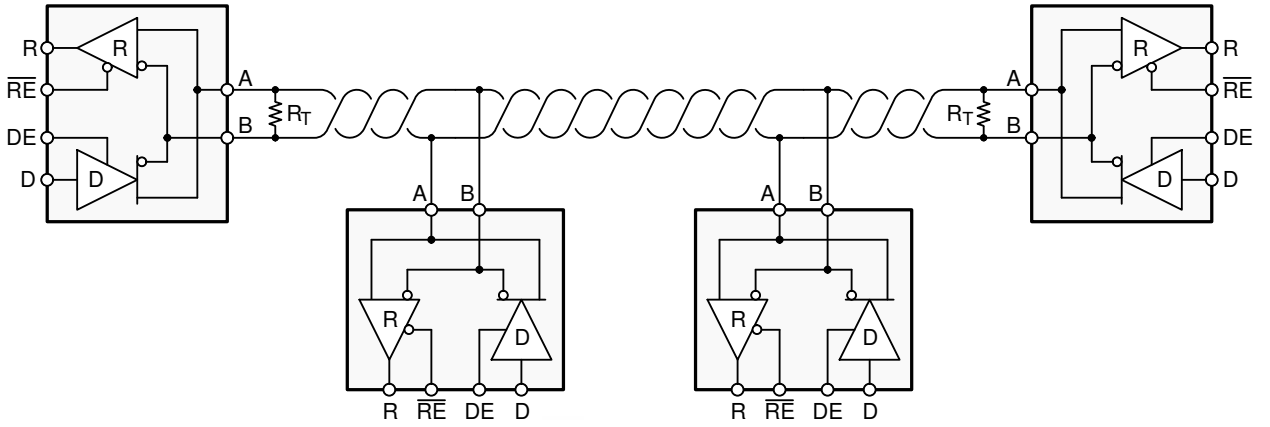


Figure 8-2. Typical RS-485 Network With Half-Duplex Transceivers

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5% or 10%.

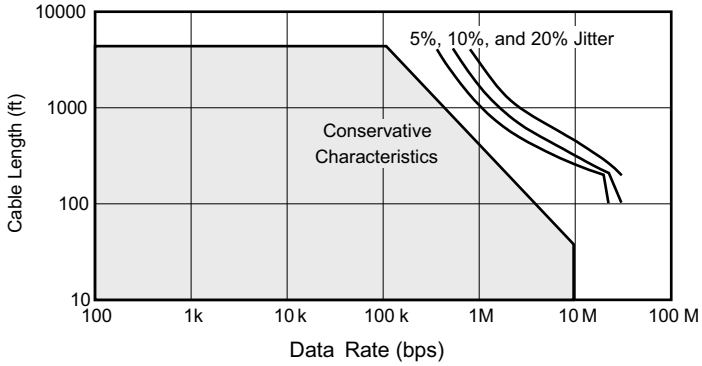


Figure 8-3. Cable Length vs Data Rate Characteristic

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- v is the signal velocity of the cable or trace as a factor of c
- c is the speed of light (3×10^8 m/s)

Per Equation 1, cable-stub lengths when using the SN65LBC184 driver must be not greater than 5.85 meters (19 feet) for a signal velocity of 78% and minimum driver output rise or fall time of 250ns.

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the SN65LBC184 is a 1/4 UL transceiver, it is possible to connect up to 128 receivers to the bus.

8.2.2 Detailed Design Procedure

8.2.2.1 SN65LBC184 Test Description

The SN65LBC184 is tested against the IEC 61000-4-5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50µs open-circuit voltage waveform and a 8-/20µs short-circuit current waveform shown in Figure 8-4. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2Ω. The setup for the overvoltage stress is shown in Figure 8-5 with all testing performed with power applied to the SN65LBC184 circuit.

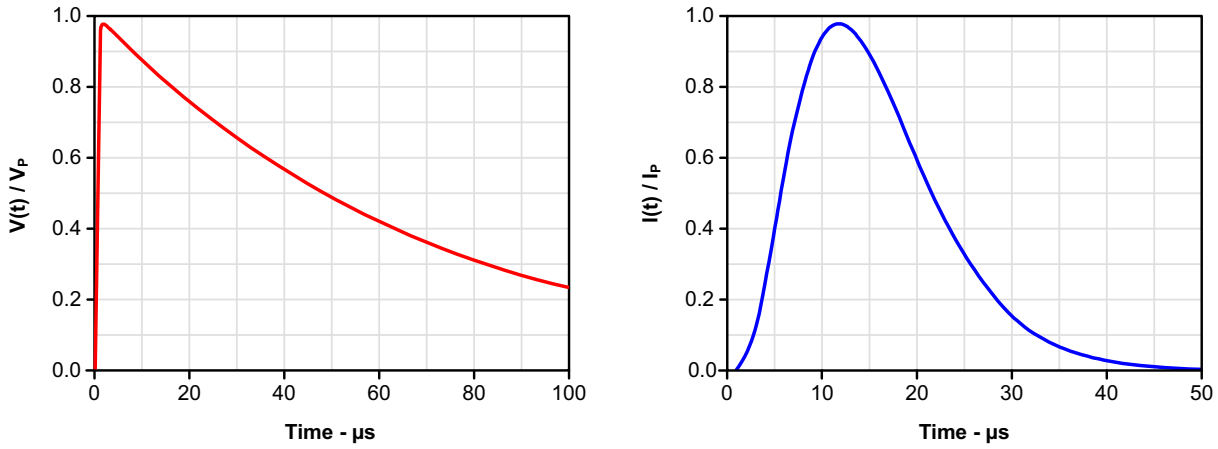


Figure 8-4. Open-Circuit Voltage and Short-Circuit Current Waveforms

The SN65LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The SN65LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A and B) across ground as shown in Figure 8-5.

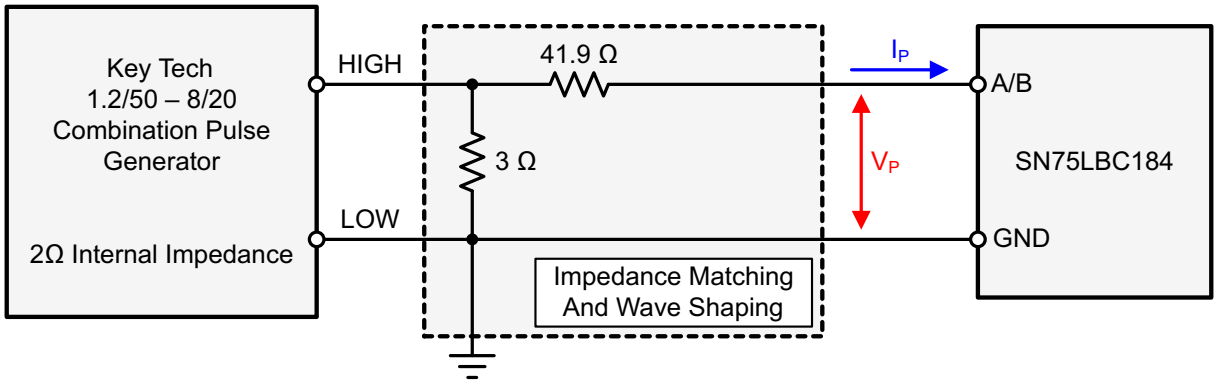


Figure 8-5. Overvoltage Stress Test Circuit

8.2.3 Application Curve

An example waveform as seen by the SN65LBC184 is shown in Figure 8-6. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 33.6V and peak current of 16A, thus yielding an absorbed peak power of 538W.

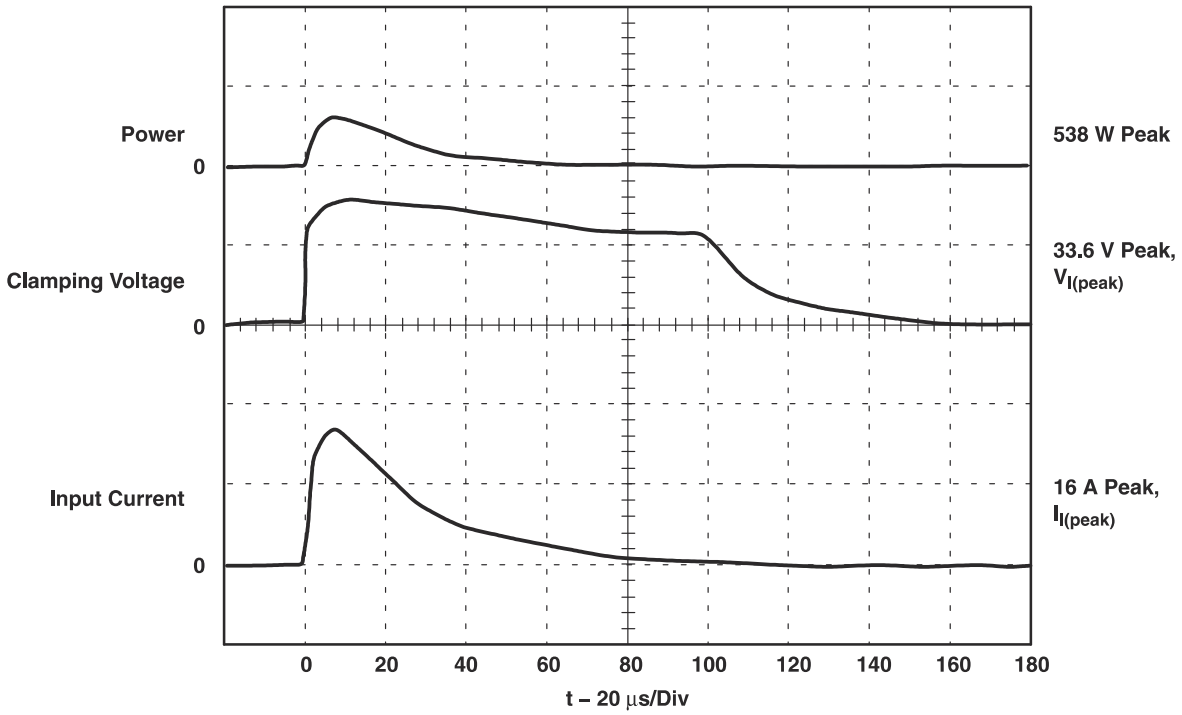


Figure 8-6. Typical Surge Waveform Measured at Pins 5 and 7

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be buffered with a 100nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 is a linear voltage regulator suitable for the 5V supply.

8.4 Layout

8.4.1 Layout Guidelines

Because ESD transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design.

- Use V_{CC} and ground planes to provide low inductance. High frequency currents follow the path of least inductance and not the path of least impedance.
- Apply 100nF to 220nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, or controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors to minimize effective via-inductance.
- Use 1kΩ to 10kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.

8.4.2 Layout Example

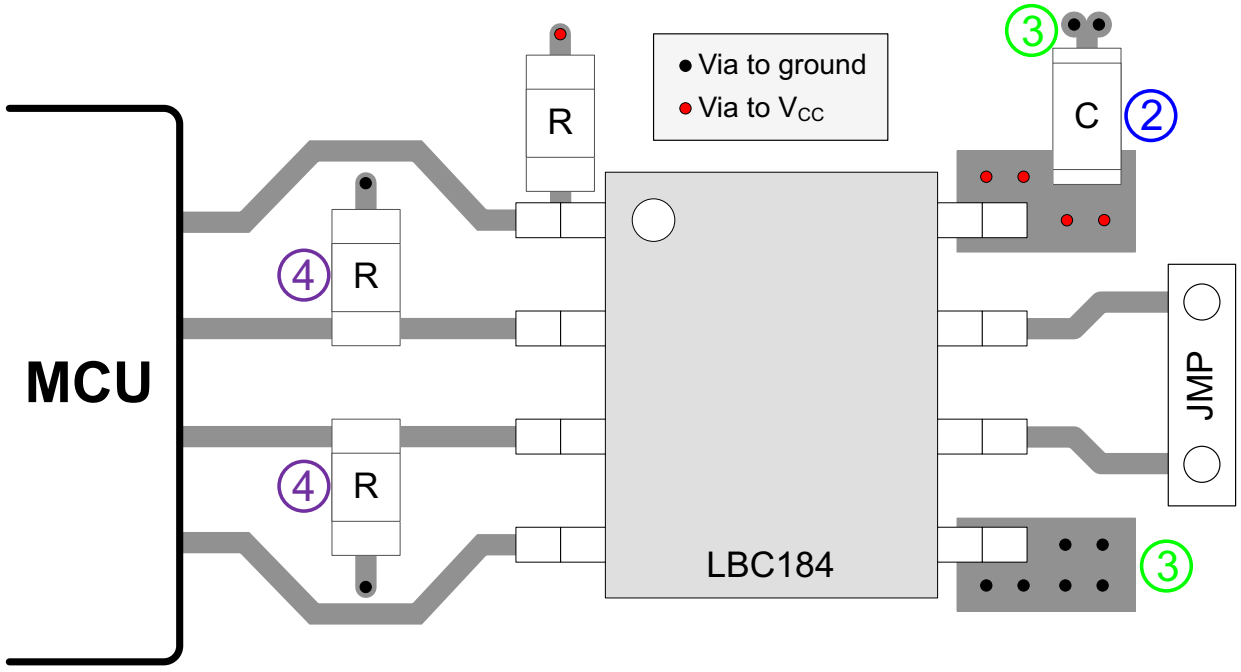


Figure 8-7. Layout Schematic

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (June 2015) to Revision J (July 2024)	Page
• Changed *Features* From: ±15 kV IEC 61000-4-2, Air-gap discharge To: ±30 kV IEC 61000-4-2, Air-gap discharge	1
• Changed the value of "Air discharge" From: ±15000 To: ±30000 in the *ESD Ratings* table	4
• Changed the D (SOIC) *Thermal Information* values	5
• Changed the V_{IT+} unit value From: 200 V To: 200 mV in the *Electrical Characteristics: Receiver* table	6

Changes from Revision H (February 2009) to Revision I (June 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC184DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6LB184, SLB18U)
SN65LBC184DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6LB184, SLB18U)
SN65LBC184DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6LB184, SLB18U)
SN65LBC184DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(6LB184, SLB18U)
SN65LBC184P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC184
SN65LBC184P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC184
SN75LBC184D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	7LB184
SN75LBC184P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC184
SN75LBC184P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC184

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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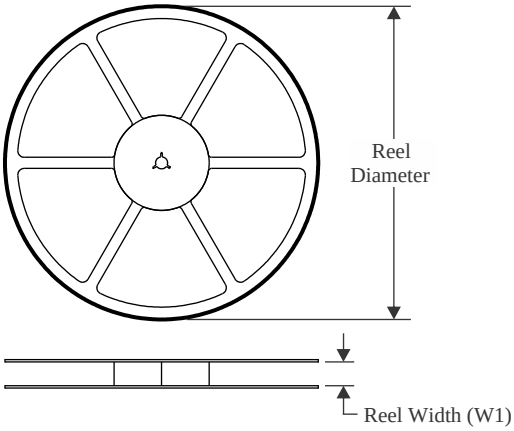
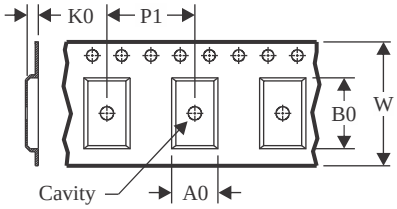
TAPE AND REEL INFORMATION

REEL DIMENSIONS

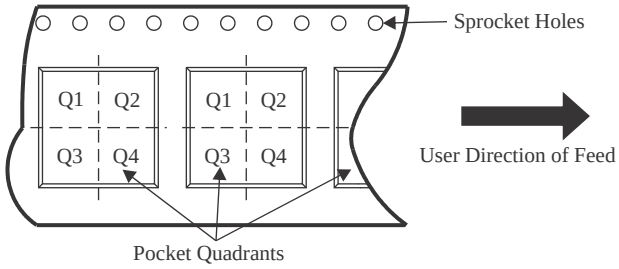


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

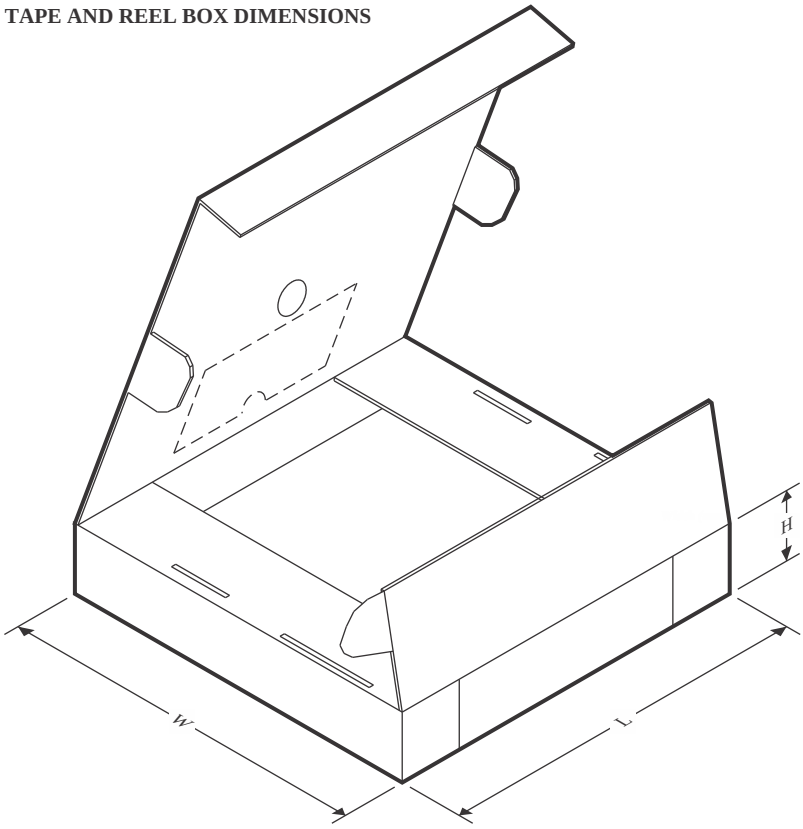
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC184DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

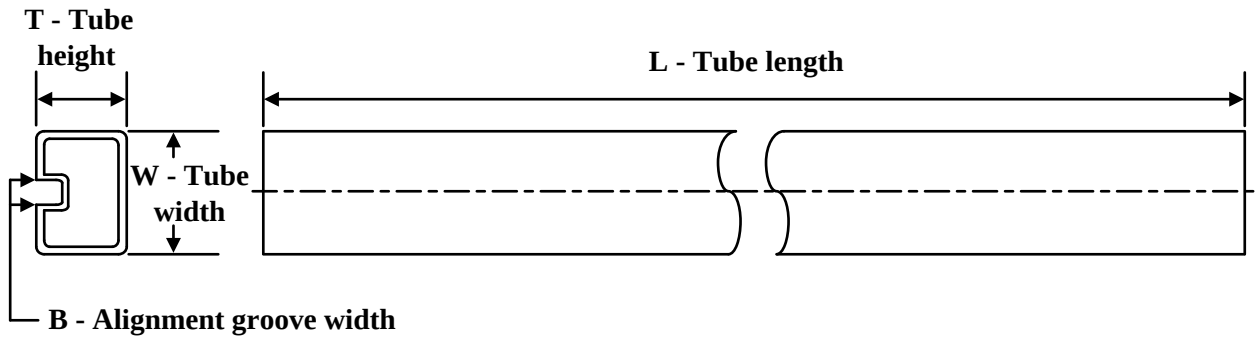
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

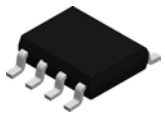
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC184DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC184P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC184P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC184P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC184P.A	P	PDIP	8	50	506	13.97	11230	4.32

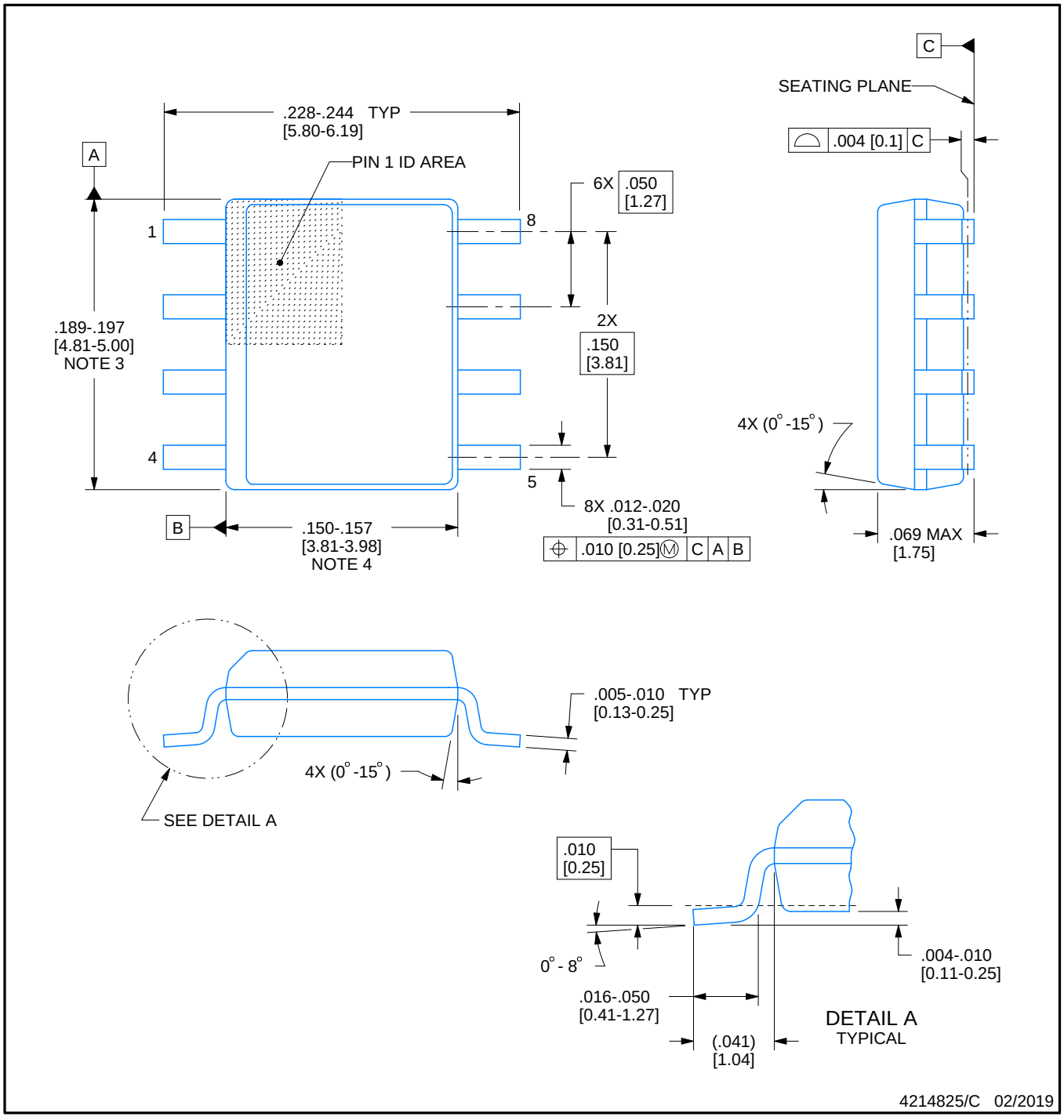


PACKAGE OUTLINE

D0008A

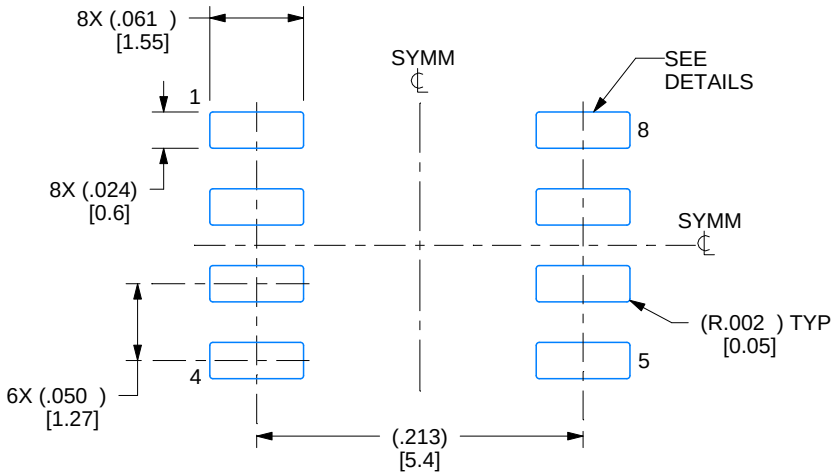
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

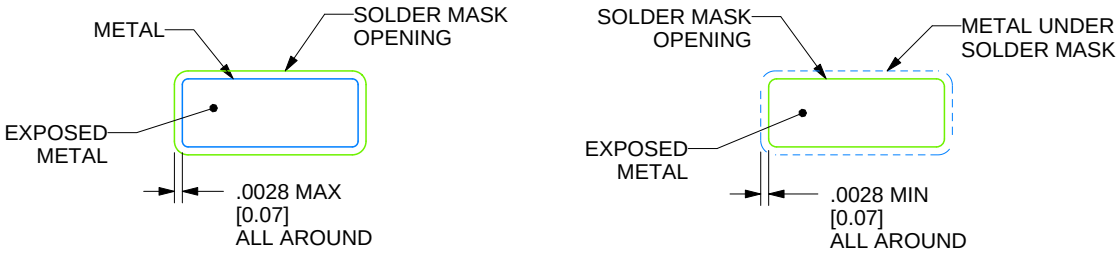


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

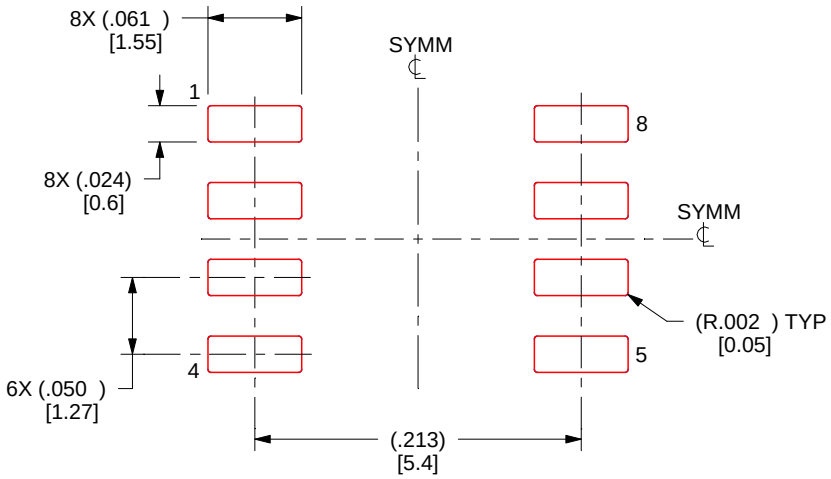
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



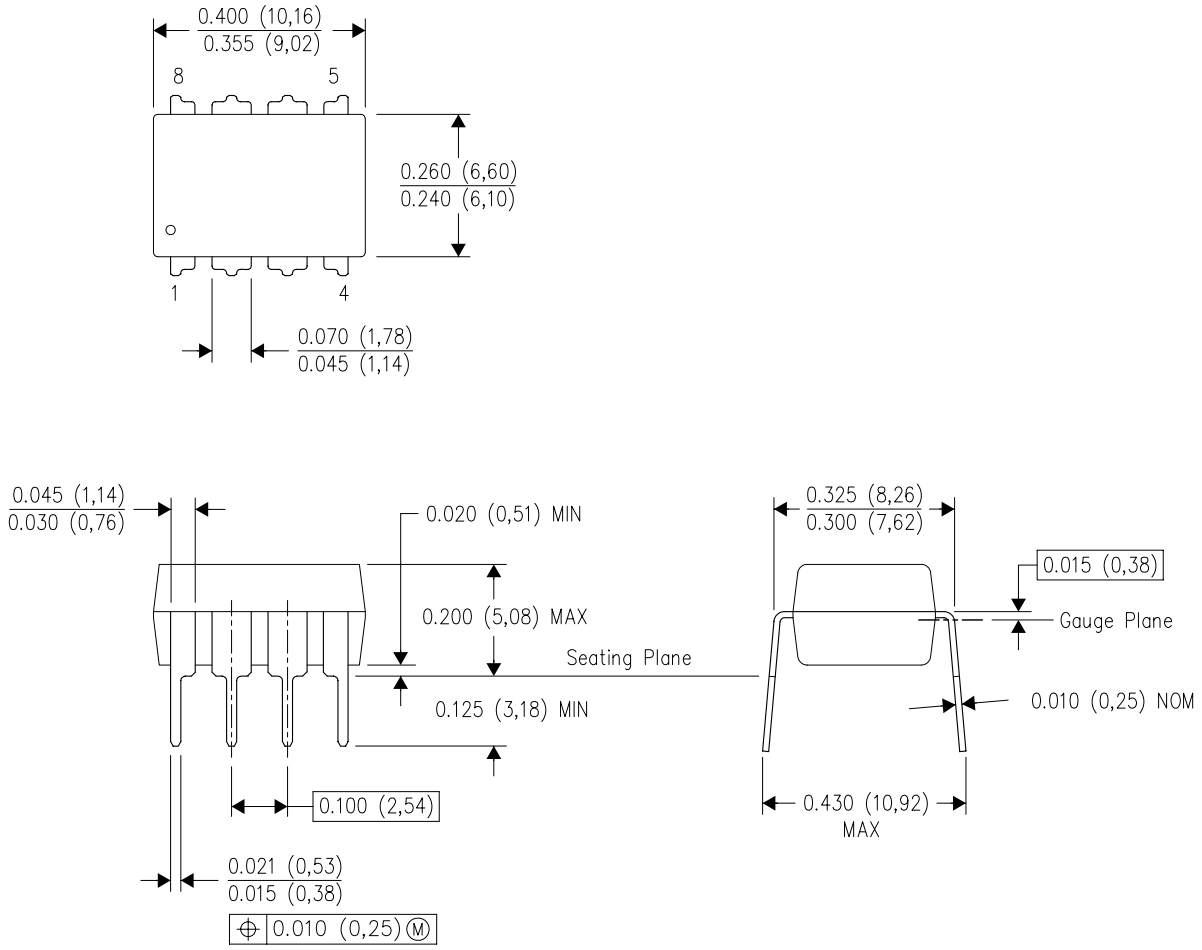
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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