4.5V~100V, 460KHz, Step-Down Converter

1 Features

- 4.5V to 100V Wide Operational Range
- Integrated High Side Power MOS with 900mΩ Low Resistance
- Constant-On-Time Control
- Low Quiescent Current: 180μA
- Low Shutdown Current: 3μA
- 460kHz Switching Frequency
- Valley Current Limiting for Non-Synchronous Buck Topology
- Float EN Pin for Automatically Start-Up
- Low Drop Out Mode Support 97% Duty Cycle
- Reference Voltage: 0.78V
- Short Circuit Protection with Hiccup Mode
- Over Temperature Protection
- Available in SOT23-6 package

2 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications

3 Description

The GD30DC1801 is a user-friendly non-synchronous buck converter, integrated with a 900mΩ low RDS_ON high-side MOSFET.

It delivers up to 1A continuous output current, employing advanced constant-on-time (COT) control for fast transient response and simplified loop compensation. With a typical switching frequency of 460kHz, the GD30DC1801 helps reduce solution size and lowers BOM cost.

The GD30DC1801 featuring a wide input voltage range of 4.5V to 100V, which accommodates a variety of step-down applications.

The GD30DC1801 built-in protection mechanisms include cycle-by-cycle current limit, hiccup-mode short-circuit protection, and thermal shutdown to safeguard against excessive power dissipation.

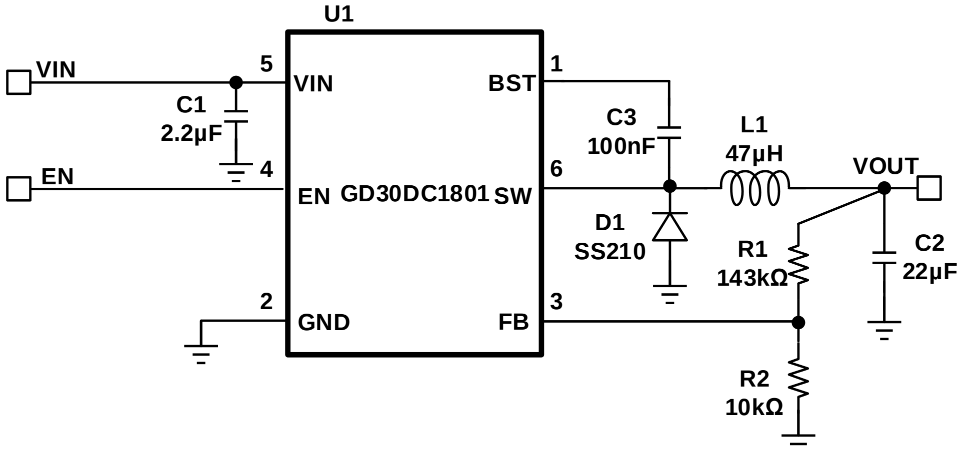
The GD30DC1801 comes in a cost-efficient SOT23-6 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1801	SOT23-6	1.60mm x 2.90mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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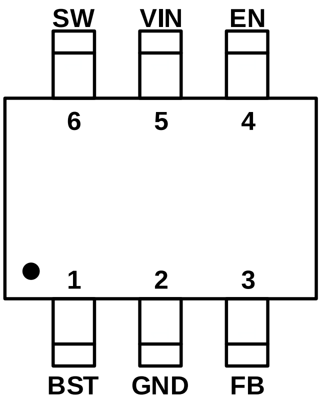
4 Device Overview

4.1 Pinout and Pin Assignment

SOT23-6
(Top View)



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	SOT23-6		
BST	1	O	**Bootstrap**. Connect a high-quality 100nF capacitor between SW and BST to form a floating supply across the high-side switch driver.
GND	2	G	**Ground Pin.** Chip's GND connection. Connect to the ground of the system.
FB	3	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider from VOUT to GND.
EN	4	I	**Enable**. Float this pin for automatically start-up, pull down this pin to shut down the IC.
VIN	5	P	**Power supply**. Supply input terminal to internal bias LDO and high-side FET. A decoupling capacitor is required to decouple the input.
SW	6	O	**Switch output**. Switching node of power stage. Connected to the internal MOSFET switches and inductor terminal.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL[1]	PARAMETER	MIN	MAX	UNIT
V_{IN}	VIN to GND	−0.3	105	V
V_{SW}	SW to GND	−0.3	105	V
V_{BST}-V_{SW}	BST to SW		6	V
I_{EN}	Max Input current to EN pin		100[2]	μA
All other pins		−0.3	6	V
T_{STG}	Storage temperature	−55	150	°C
T_J	Junction temperature	−40	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
2. For details on EN's ABS max rating, please refer to the Enable Control section.

5.2 Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	VIN to GND	4.5		100	V
V_{OUT}	VOUT to GND	0.8		V_{IN}*D_{MAX}[1] or V_{OUT}<24V	V
I_{OUT}	Continuous Output Current	0		1	A

1. $D_{MAX} = T_{ON\_MAX} / (T_{ON\_MAX} + T_{OFF\_MIN})$. Typical value is 97%.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	SOT23-6	40	°C/W
Θ_{JC}	Junction to case (top) thermal resistance	SOT23-6	21	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 60V and T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN_{UV_R}	VIN UVLO rising voltage		4.15	4.3	4.45	V
VIN_{UV_F}	VIN UVLO falling voltage		3.9	4.05	4.2	V
VIN_{UV_HYS}	Hysteresis voltage of VIN UVLO			0.25		V
I_S	Shut down current from VIN	V_{EN} = 0V		3	6	µA
I_Q	Quiescent current from VIN	V_{FB} = 0.85V		180		µA
V_{EN_R}	Enable rising voltage		1.1	1.2	1.3	V
V_{EN_F}	Enable falling voltage		0.85	0.95	1.05	V
$I_{EN\_PULL\_UP}$	Enable pull-up current	V_{EN} = Low		1		µA
		V_{EN} = High		4		
V_{EN_CLAMP}	Enable clamp voltage	EN voltage at 100uA current		5.7		V
V_{FB}	Feedback voltage		0.768	0.78	0.792	V
V_{FB_UV}	Feedback UVLO threshold			0.1		V
R_{HS_ON}	High Side power MOS ON resistance	V_{BST}-V_{SW} = 5V		900		mΩ
I_{LIMIT_HS}	High side current limit threshold		1.4	1.8	2.2	A
T_{SS}	Soft-start time	V_{FB} from 10% to 90%		1.8		ms
F_{SW}	Switching frequency		400	460	557	kHz
T_{ON_MIN}[1]	Min on time			150		ns
T_{ON_MAX}	Max on time			10		µs
T_{OFF_MIN}[1]	Min off time			350		ns
T_{VALLEY_MAX}[1]	Max valley off time			100		µs
T_{OTP_R}[1]	Thermal shutdown entry threshold			160		°C
T_{OTP_F}[1]	Thermal shutdown recovery threshold			140		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

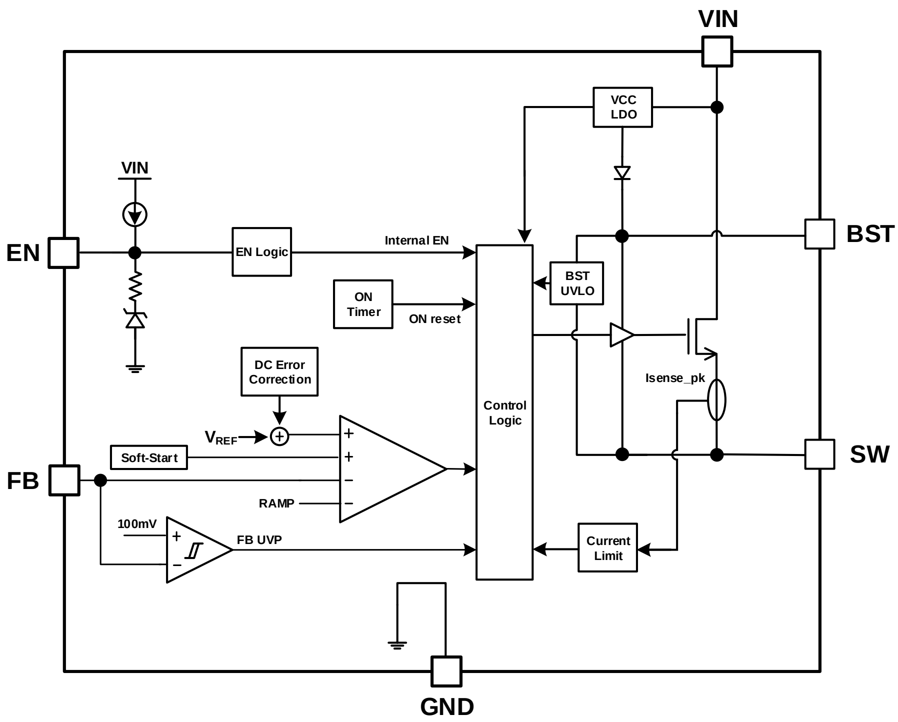


Figure 1. GD30DC1801 Functional Block Diagram

6.2 Pulse-Width Modulation (PWM) Operation

The GD30DC1801 is a fully integrated non-synchronous step-down converter. It utilizes constant-on-time (COT) control to achieve fast transient response and simplify loop stabilization. At the start of each cycle, the high-side MOSFET (HS-FET) is activated when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), signaling that the output voltage is insufficient. The on-time duration is determined by both the input and output voltages, ensuring relatively stable switching frequency across the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. Through this repetitive process, the converter regulates the output voltage.

To enhance stability, internal compensation is integrated with the COT control, enabling stable performance even when ceramic capacitors are used for output. This internal mechanism also improves jitter performance without affecting the line or load regulation.

6.2.1 Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current remains above zero amps (see Figure 2). When the V_{FB} falls below the V_{REF}, the HS-FET turns on for a fixed duration controlled by the one-shot timer. Once the HS-FET switches off, the external free-wheeling diode carries the current.

In CCM, the switching frequency remains relatively stable, a behavior known as pulse-width modulation (PWM) mode.

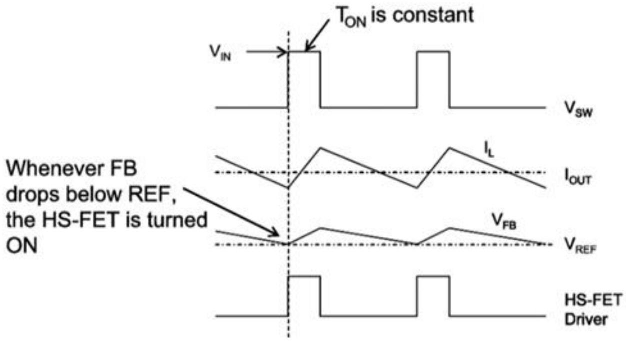


Figure 2. Heavy-Load Operation

6.2.2 Light-Load Operation

As the load decreases, the inductor current also drops. When the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load behavior is illustrated in Figure 3. When theVFB falls below the V_{REF}, the HS-FET turns on for a fixed duration determined by the one-shot timer. After the HS-FET turns off, the free-wheeling diode activates until the inductor current hits zero. In DCM, V_{FB} cannot reach V_{REF} while the inductor current approaches zero. At this point, the free-wheeling diode blocks any negative current, and the IC enters a tri-state mode. The output capacitor slowly discharges to GND via the feedback resistor, significantly enhancing efficiency during light-load conditions.In light-load mode, the HS-FET activates less frequently compared to heavy-load conditions, a behavior known as skip mode.

At light or no load, the output drops very slowly, and the GD30DC1801 naturally lowers its switching frequency, thereby achieving high efficiency during light loads.

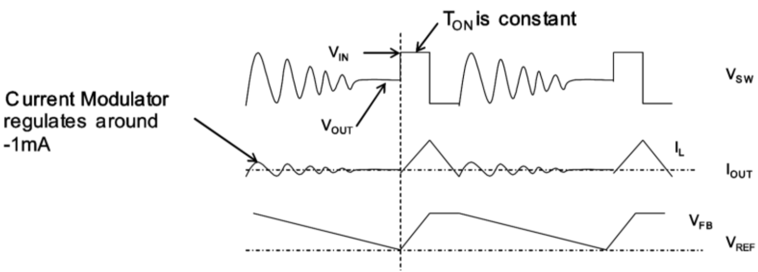


Figure 3. Light-Load Operation

As the output current rises from a light-load state, the HS-FET is activated more frequently, leading to an increase in the switching frequency. When the modulation time reduces to zero, the output current reaches the critical level. The critical output current can be calculated using the equation provided below.

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device switches to PWM mode once the output current surpasses the critical level. Afterward, the switching frequency remains relatively stable across the output current range.

6.2.3 Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) feature ensures the chip does not operate at inadequate supply voltages. The GD30DC1801's UVLO comparator monitors the input voltage, with a rising threshold of approximately 4.3V and a falling threshold of 4.05V.

6.2.4 Enable (EN) Control

The GD30DC1801 includes a dedicated enable control pin with positive logic. To activate the regulator, apply a voltage above 1.2V (typical) to the EN pin, and to disable it, set the EN pin voltage below 0.95V (typical).

The EN pin includes an internal 4μA pull-up current source, enabling the GD30DC1801 to automatically start up when the EN pin is left floating.

To shut down the regulator via the EN pin, a pull-down current greater than 4μA is required. Once the EN pin is pulled low, the internal pull-up current reduces to 1μA, minimizing the shutdown current.

By using two external resistor dividers, the start and stop voltages of the system can be easily optimized via the EN pin.

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 0.95 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (3)$$

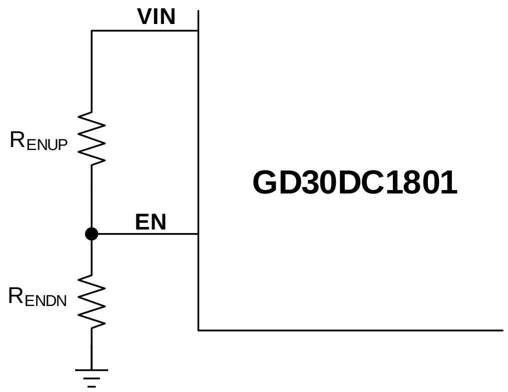


Figure 4. EN divider for adjustable UVLO

6.2.5 Internal Soft Start (SS)

The soft-start (SS) function prevents output voltage overshoot during start-up. When the chip powers on, the internal circuit generates a soft-start voltage (V_{SS}) that gradually increases from 0V to 1V. While V_{SS} remains below V_{REF}, V_{SS} replaces V_{REF} as the reference for the error amplifier. Once V_{SS} surpasses V_{REF}, the error amplifier switches back to using V_{REF}. The soft-start duration is internally set to 1.8ms.

6.2.6 High Duty Mode Operation

The GD30DC1801 automatically extend the on time to support the application when V_{IN} is close to V_{OUT}. The on time extend circuit will be triggered when T_{OFF_MIN} time is reached. The GD30DC1801 can support up to 97% maximum duty cycle.

6.2.7 Current Limit and Short Protection

The GD30DC1801 features both a peak current limit and a unique valley current limit. While the HS-FET is on, the inductor current is monitored. If the sensed inductor current exceeds the peak current limit after the blanking time, the HS-FET turns off. However, in a non-synchronous buck configuration, the inductor current might increase uncontrollably during output short-circuit conditions due to the blanking time. GD30DC1801 utilizes a special valley current limit to prevent this issue. When the HS-FET is off and the inductor current exceeds the valley current limit, the HS-FET remains off until the output current falls below the valley current limit threshold.

In cases where the output is shorted to ground, the GD30DC1801 automatically reduces the switching frequency to prevent current runaway, enhancing system reliability.

6.2.8 Thermal Shutdown

The thermal shutdown feature protects the chip from excessive temperatures. If the silicon die temperature exceeds 160°C, the chip automatically powers down. It reactivates once the temperature drops below the lower threshold, typically 140°C.

7 Application Information

7.1 Typical Application Circuit

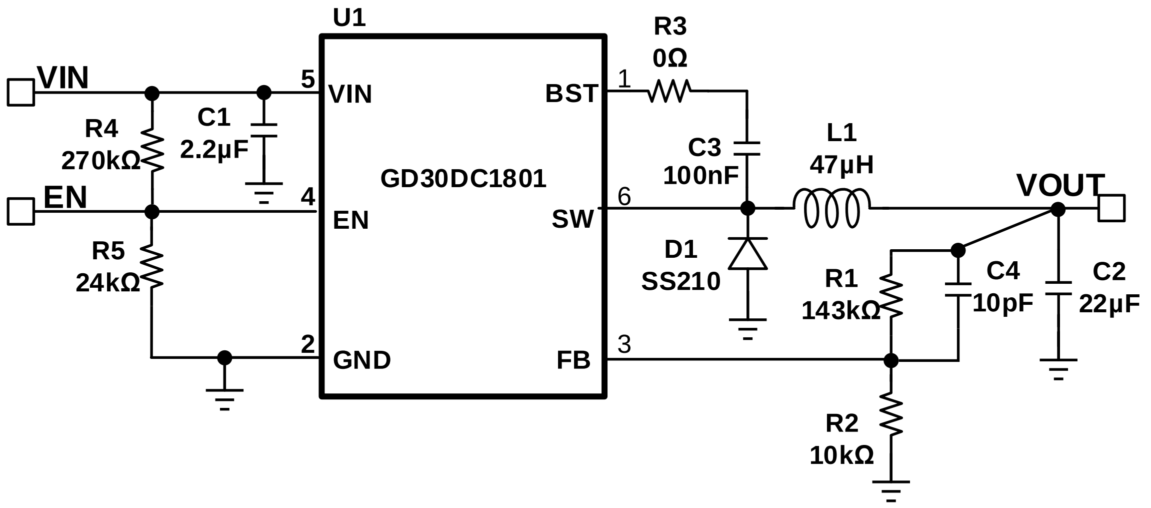


Figure 5. V_{IN}=48V, V_{OUT}=12V/1A

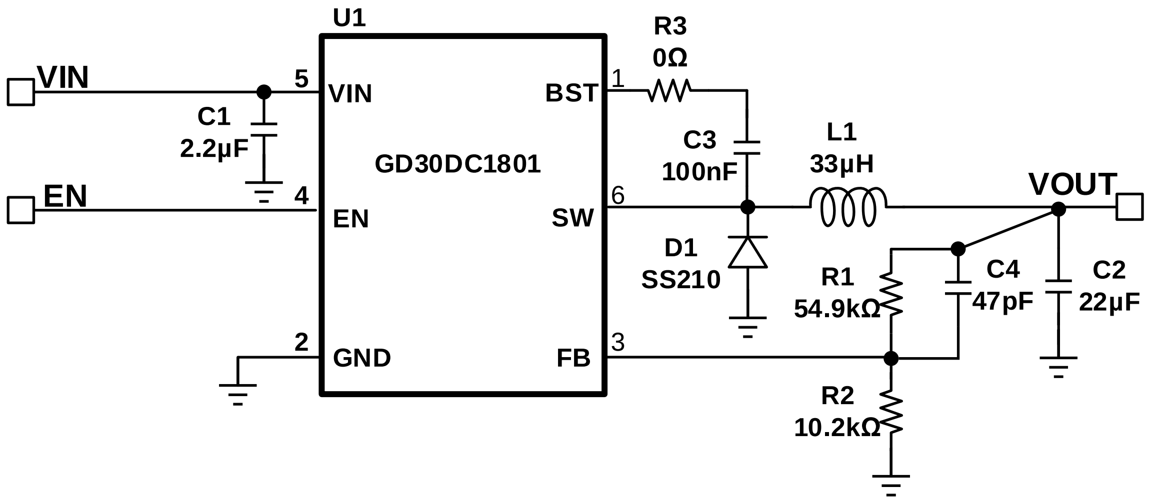


Figure 6. V_{IN}=48V, V_{OUT}=5V/1A

7.2 Detailed Design Description

7.2.1 Setting the Output Voltage

The GD30DC1801 output voltage is configured via external resistor dividers, with a fixed reference voltage of 0.8V. The feedback network layout is shown in the figure below.

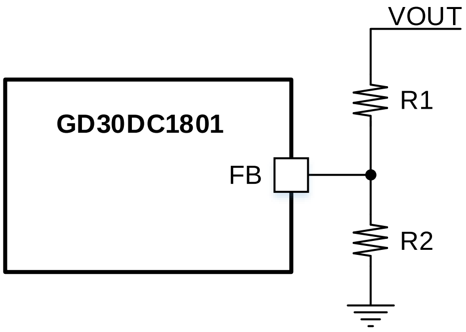


Figure 7. Feedback resistor divider

Choose R1 and R2 using Equation(4):

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \tag{4}$$

7.2.2 Selecting the Inductor

An inductor is essential for providing continuous current to the load while being driven by the switched input voltage. A larger inductor minimizes ripple current and reduces output voltage ripple but comes with drawbacks such as a larger physical size, higher series resistance, and lower saturation current. For most designs, the suitable inductance value can be calculated using the following Equation(5):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \tag{5}$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation(6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \tag{6}$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1. Resistor Selection for Common Output Voltages[1]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff} (pF)	L (μH)	C_{OUT} (μF)
12	143	10	10	47	22
5	54.9	10.2	47	33	22

1. For a detailed design circuit, please refer to the Typical Application Circuits

7.2.3 Selecting the Output Capacitor

The output capacitor (C2, C3) are responsible for maintaining the DC output voltage ripple. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred for minimizing output voltage ripple, which can be estimated using the Equation(7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also influence the stability of the regulation system. The GD30DC1801 is designed to operate efficiently across a wide range of capacitance and ESR values.

7.3 Typical Characteristics

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

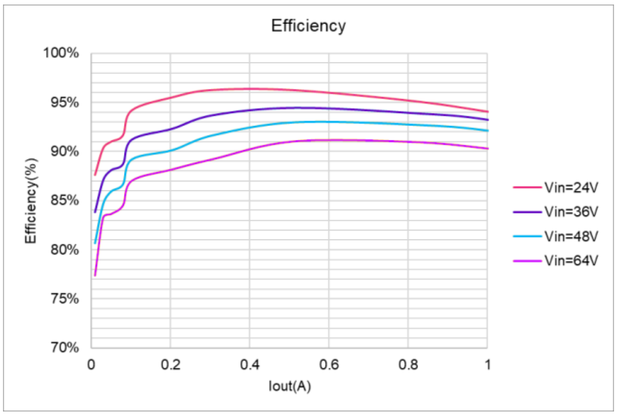


Figure 8. Efficiency vs. Load Current(V_{OUT}=12V, L=47μH, DCR=135mΩ)

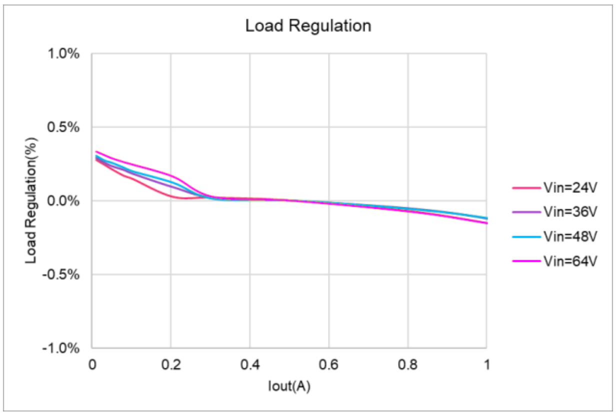


Figure 9. Load Regulation

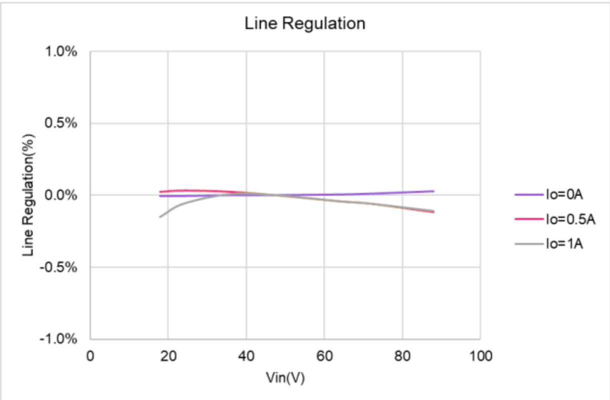


Figure 10. Line Regulation

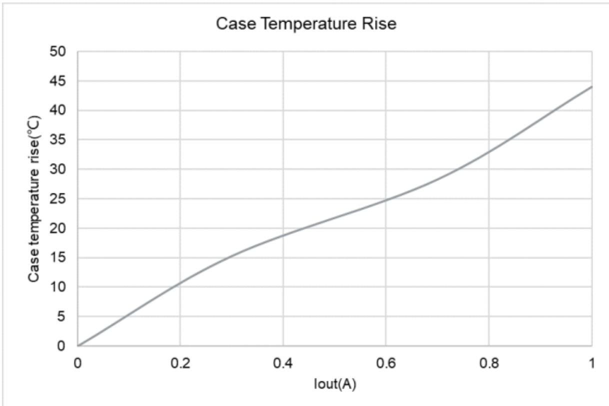


Figure 11. Thermal Rise (V_{OUT} = 12V, no air flow)

Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

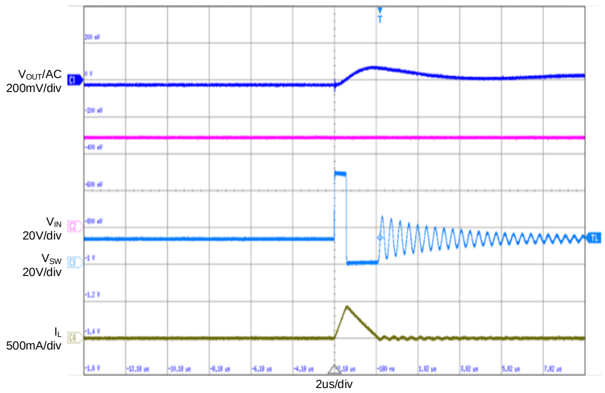


Figure 12. Output Voltage Ripple (I_{OUT}=0A)

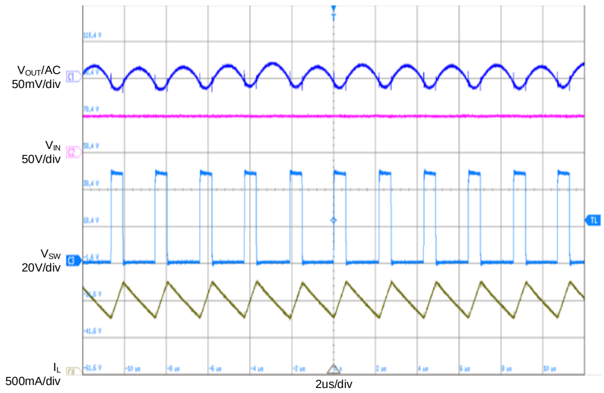


Figure 13. Output Voltage Ripple (I_{OUT}=1A)

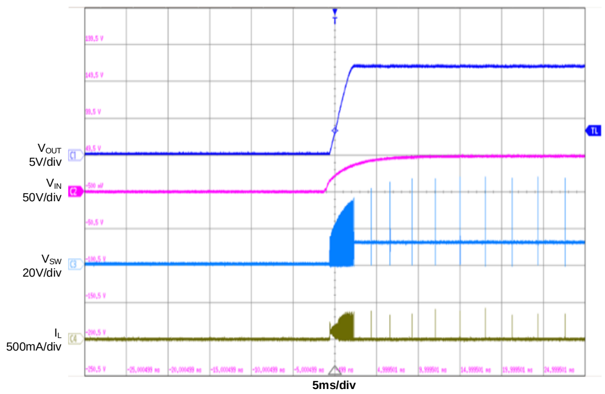


Figure 14. Startup through V_{IN} (I_{OUT} = 0A)

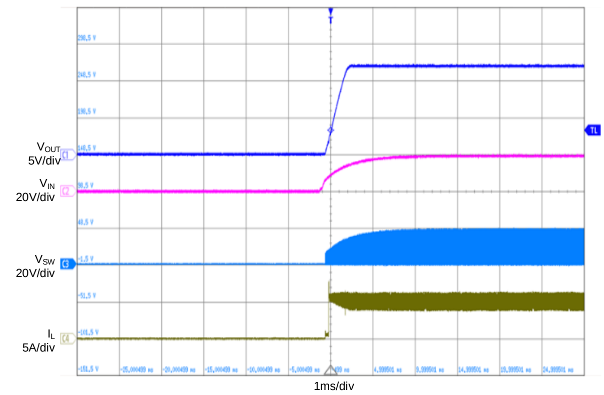


Figure 15. Startup through V_{IN} (I_{OUT} = 1A)

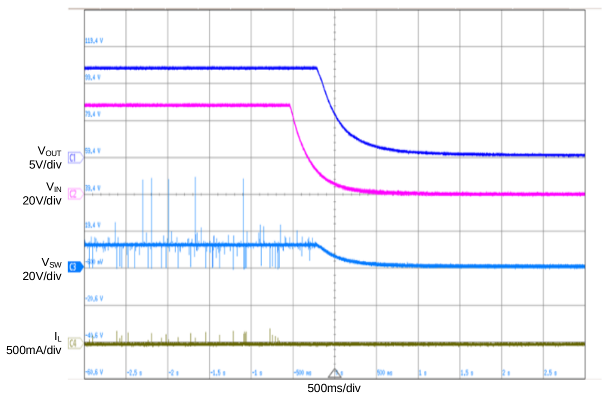


Figure 16. Shutdown through V_{IN} (I_{OUT} = 0A)

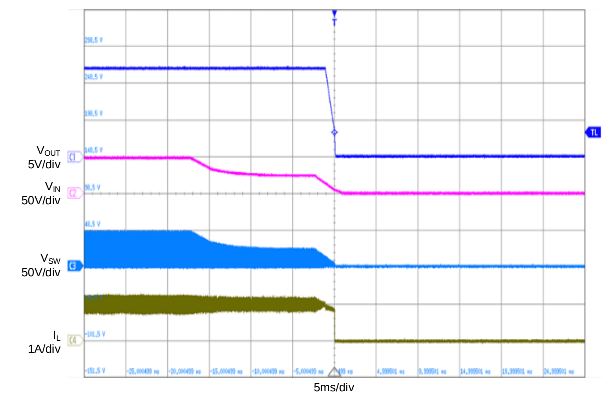


Figure 17. Shutdown through VIN (I_{OUT} = 1A)

Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2µF, C_{OUT} = 22µF, L1 = 47µH, and T_A = +25°C, unless otherwise noted.

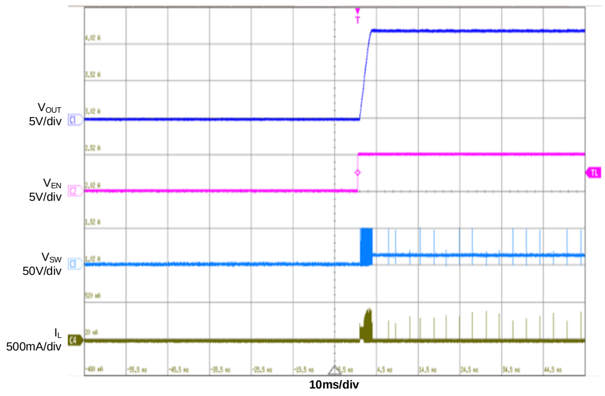


Figure 18. Startup through EN (I_{OUT} = 0A)

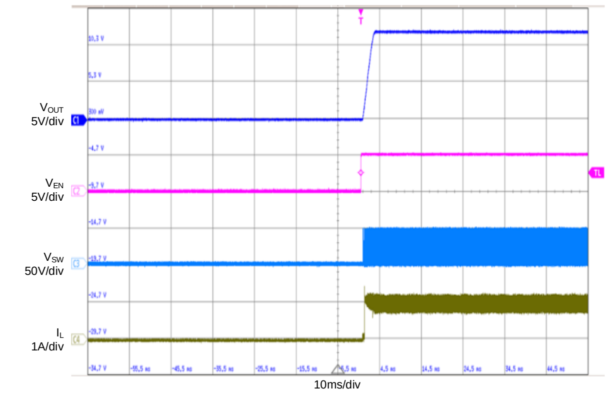


Figure 19. Startup through EN (I_{OUT} = 1A)

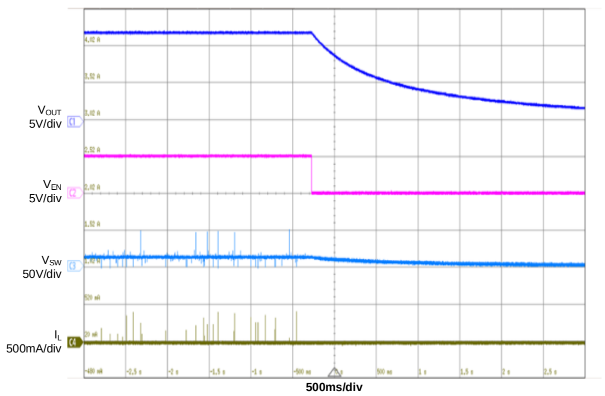


Figure 20. Shutdown through EN (I_{OUT} = 0A)

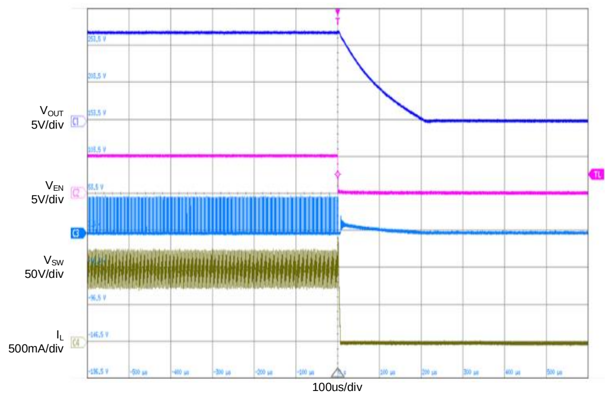


Figure 21. Shutdown through EN (I_{OUT} = 1A)

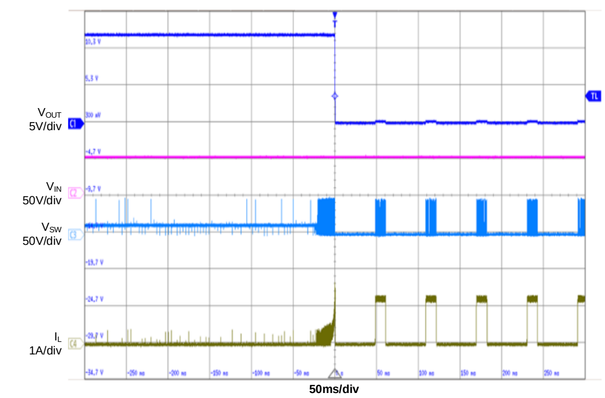


Figure 22. SCP Entry (I_{OUT} = 0A)

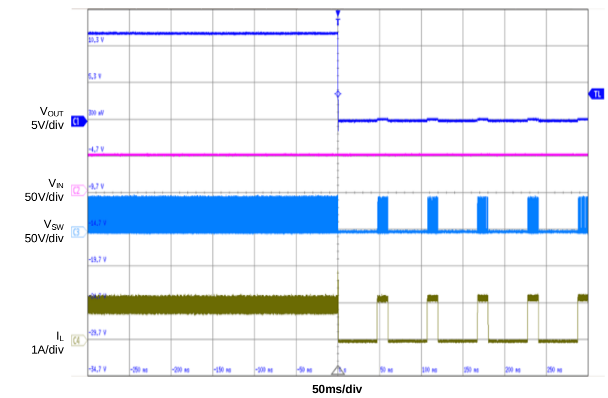


Figure 23. SCP Entry (I_{OUT} = 1A)

Typical Characteristic (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

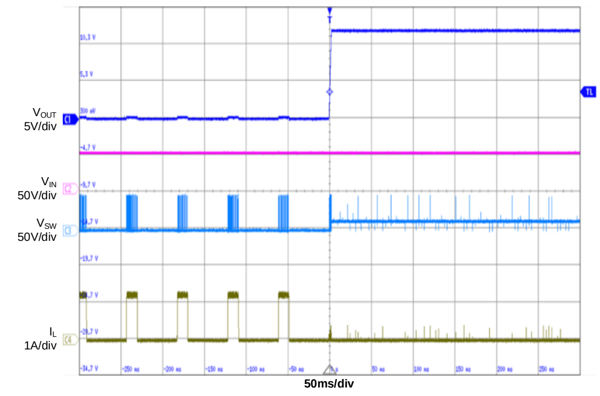


Figure 24. SCP Recovery (I_{OUT} = 0A)

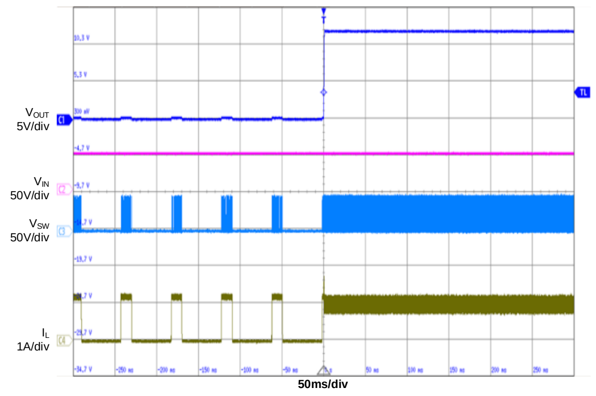


Figure 25. SCP Recovery (I_{OUT} = 1A)

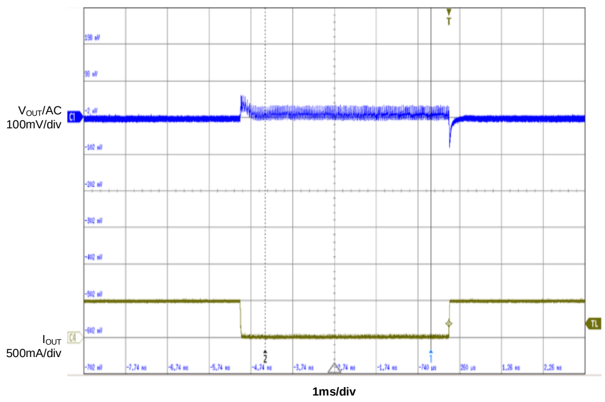


Figure 26. Load Transient (V_{OUT}=5V, L=33μH, I_{OUT} = 0.01A to 0.5A, 2.5A/μs Slew Rate)

8 Layout Guidelines and Example

Proper layout design is essential for the stable operation of switching power supplies. In high-frequency switching converters, poor layout can lead to issues such as unstable operation and poor line or load regulation. For optimal performance, refer to the figure below and follow these guidelines:

1) Place the input capacitor as close to V_{IN} and GND as possible.
2) Position external feedback resistors near the FB pin for best accuracy.
3) Keep the switching nodes (e.g., SW and BST) away from the feedback network to reduce interference.
4) Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.

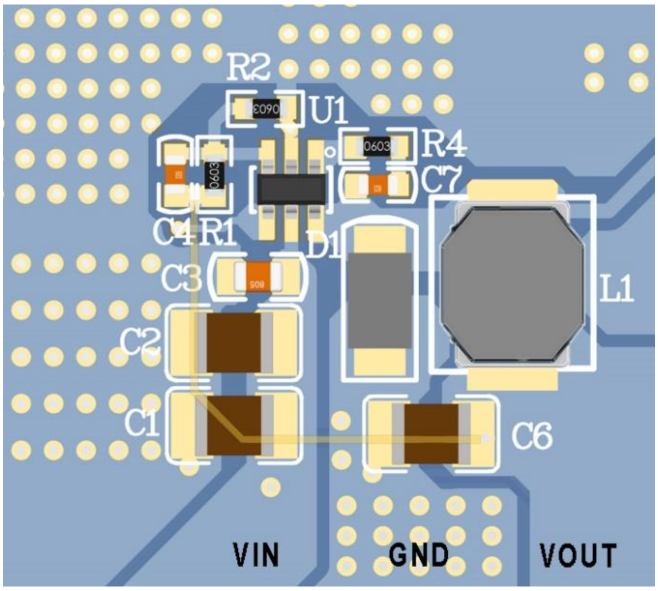
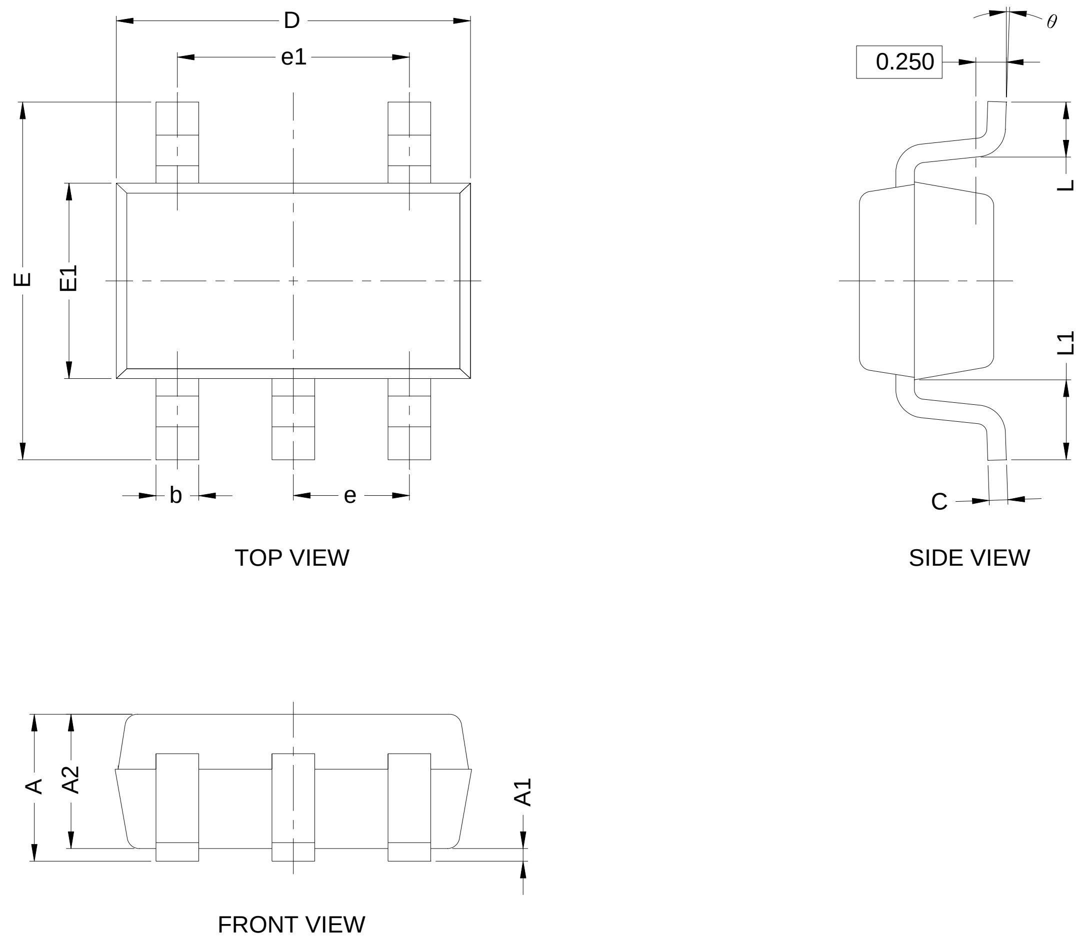


Figure 27. Typical GD30DC1801 Example Layout

9 Package Information

SOT23-6 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 2 *SOT23-6 dimensions(mm)*.

Table 2. SOT23-6 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.45
A1	0		0.15
A2	0.90	1.10	1.30
b	0.30		0.50
c	0.09		0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1801NSTR-I	SOT23-6	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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