4.5V~100V, 3.8A Peak Current Limit Step-Down Converter

1 Features

- 4.5V to 100V Wide Operational Range
- Peak Current Limit: 3.8A Typical
- Integrated High Side Power MOS with 500mΩ Low Resistance
- Constant On Time Control
- 150kHz/240kHz/460kHz Switching Frequency Selectable
- Special Valley Current Limit for Non-Sync Buck Short Protection
- Low Quiescent Current: 190μA
- Low Current at Off-state: 3μA
- Built-in Pull-up Current at EN Pin
- Full Protection: Over Current Protection, Output Over Voltage Protection, FB Open/Short Protection, Over Temperature Protection
- Available in ESOP8 package

2 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications
- GPS tracker

3 Description

The GD30DC1803 is a 100V/ 3.8A peak switching current limit, non-sync buck converter.

The GD30DC1803 integrated with high-side power MOSFET with advanced COT control method, the size of the total solution will be small, load transient will be excellent, and also with good robustness.

Integrated BST charge circuit minimize the cost and solution size. High duty on-time extension make the part ideal for the application that need low drop-out feature.

190μA quiescent current saves the power, and 3μA low off current is good for those battery powered applications.

With 4.5V to 100V wide input voltage range, the GD30DC1803 accommodates a variety of step-down applications.

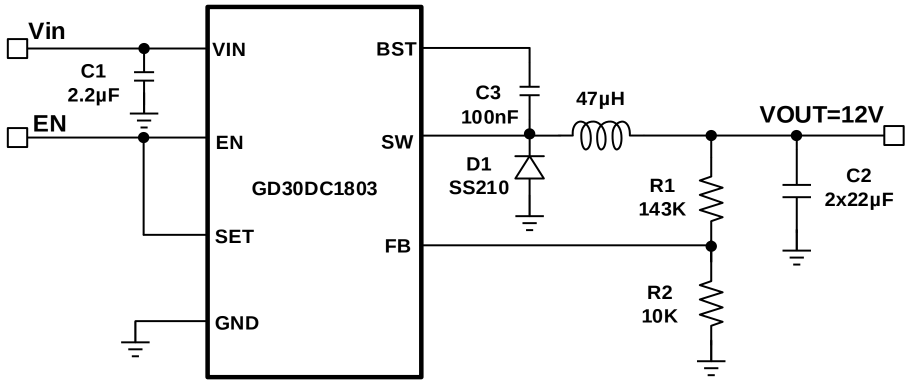
The GD30DC1803 is available in a cost-effective ESOP8 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1803	ESOP8	4.90mm x 3.90mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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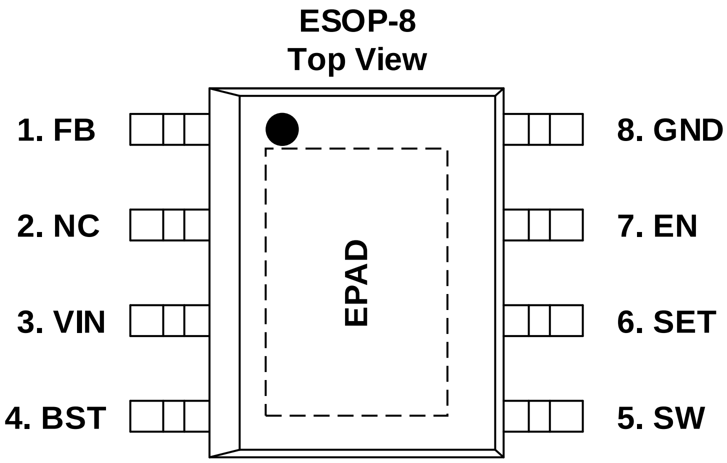
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	ESOP8		
FB	1	I	**Feedback input**. Connect a resistor divider to set the output voltage.
NC	2		No connection pin for GD30DC1803.
VIN	3	P	**Input Supply Pin**. Supply input terminal to internal bias LDO and high-side FET. A decoupling capacitor is required to decouple the input.
BST	4	O	**Bootstrap**. Connect a high-quality 100nF capacitor between SW and BST to form a floating supply across the high-side switch driver.
SW	5	O	**Switch output**. Switching node of power stage. Connected to the internal MOSFET switches and inductor terminal.
SET	6	I	**Switching frequency set pin**. Place an resistor from this pin to GND to set the IC switching frequency, float this pin or connect it to EN pin directly to set 420kHz switching frequency.
EN	7	I	**Enable pin**. Float to enable GD30DC1803. Pull down this pin to shut down the part. Internally pulled up by 4μA current.
GND	8	G	**Ground pin**. Connect to the power ground of the system.
EPAD	9	G	**Exposed Pad**. Connect exposed pad to the PCB GND plane to achieve good thermal performance.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	V_{IN} to GND	−0.3	105	V
V_{SW}	V_{SW} to GND	−0.6	105	V
V_{BST}-V_{SW}	V_{BST} to V_{SW}		6	V
I_{EN}	Max Input current to EN pin		100[2]	μA
All other pins		−0.3	6	V
T_{STG}	Storage temperature	−55	150	°C
T_J	Junction temperature	−40	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
2. For details on EN's ABS max rating, please refer to the *Enable (EN) Control* section.

5.2 Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	V_{IN} to GND	4.5		100	V
V_{OUT}	Output voltage	0.8		V_{IN}*D_{MAX}[1] or V_{OUT}<30V	V
I_{OUT_DC}	Max Continuous Output Current (V_{OUT}=12V)	0		1.5	A
	Max Continuous Output Current (V_{OUT}=5V)	0		2	A
I_{OUT_AC}	Transient Output Current	0		3	A

1. $D_{MAX} = T_{ON\_MAX} / (T_{ON\_MAX} + T_{OFF\_MIN})$. Typical value is 97%.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	ESOP8	48	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	ESOP8	52	°C/W
$\Theta_{JC(BOT)}$	Junction to case (bottom) thermal resistance	ESOP8	2.3	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 60V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO and QUIESCENT CURRENT						
VIN_{UV_R}	VIN UVLO rising threshold		4.15	4.3	4.45	V
VIN_{UV_F}	VIN UVLO falling threshold		3.9	4.05	4.2	V
VIN_{UV_HYS}	VIN UVLO hysteresis			0.25		V
I_S	Shut down current from VIN	V_{EN}=0V		3	6	μA
I_Q	Quiescent current from VIN	V_{FB}=0.85V		190		μA
ENABLE						
V_{EN_R}	Enable rising voltage		1.1	1.2	1.3	V
V_{EN_F}	Enable falling voltage		0.85	0.95	1.05	V
$I_{EN\_PULL\_UP}$	Enable pull-up current	V_{EN}=Low		1		μA
		V_{EN}=High		4		
V_{EN_CLAMP}	Enable clamp voltage	EN voltage at 100uA current		5.7		V
FEEDBACK						
V_{FB}	Feedback voltage		0.768	0.78	0.792	V
V_{FB_UV}	Feedback UVLO threshold			0.14		V
POWERSTAGE						
R_{HS_ON}	High Side power MOS ON resistance	V_{BST}-V_{SW}=5V		500		mΩ
CURRENT LIMIT						
I_{LIMIT_HS}	High side current limit threshold		3	3.8	4.5	A
SOFT START						
T_{SS}	Soft-start time	V_{OUT} from 10% to 90%		1.8		ms
SWITCHING FREQUENCY						
F_{SW}	Switching frequency	SET pin float or connected to EN pin	400	460	557	KHz
		R_{SET} = 150K	200	240	320	
		R_{SET} = 75K	120	150	205	
T_{ON_MIN}[1]	Min on time			150		ns
T_{ON_MAX}	Max on time			10		μs

Electrical Characteristics (continued)

V_{IN} = 60V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{OFF_MIN}[1]	Min off time			320		ns
THERMAL PROTECTION						
T_{OTP_R}[1]	Thermal shutdown entry threshold			160		°C
T_{OTP_F}[1]	Thermal shutdown recovery threshold			140		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

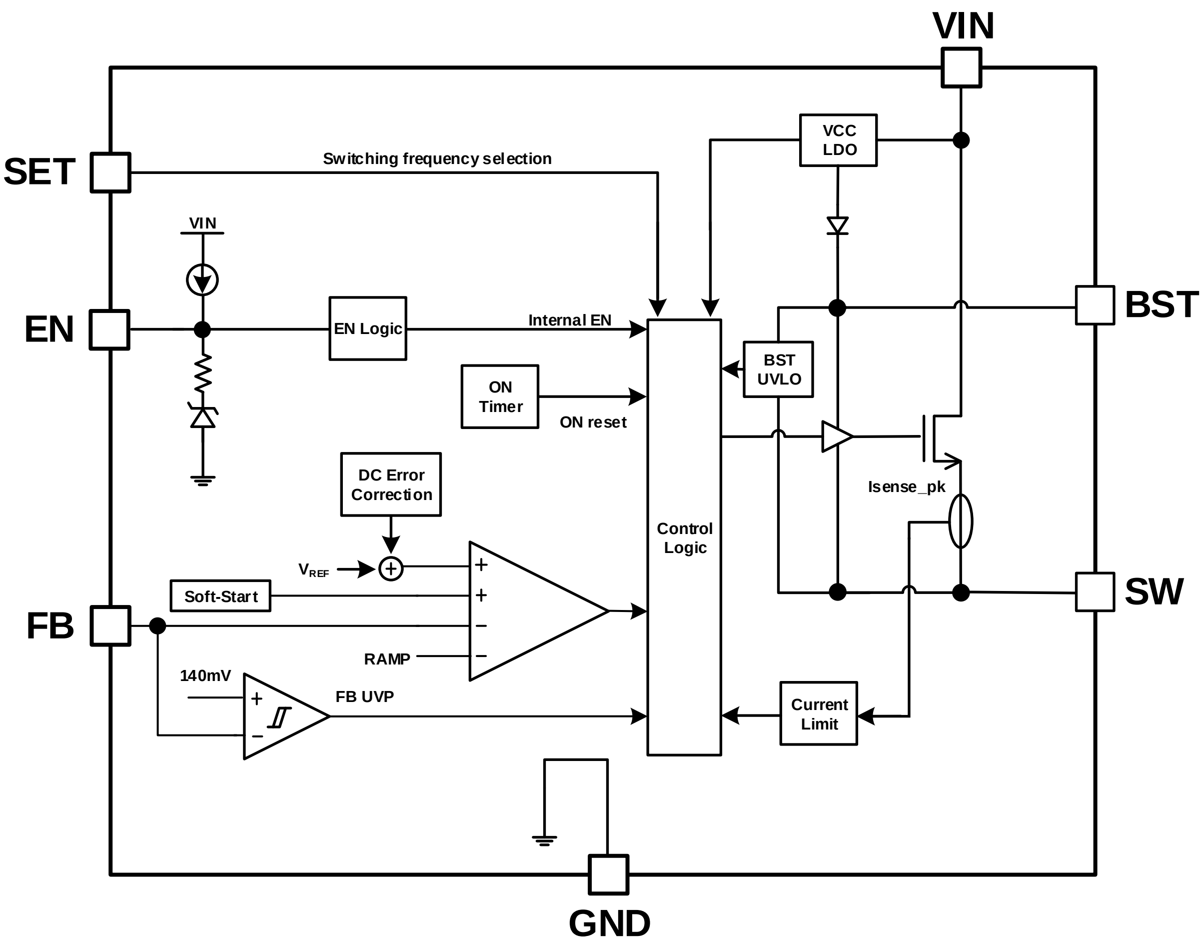


Figure 1. GD30DC1803 Functional Block Diagram

6.2 Pulse-Width Modulation (PWM) Operation

The GD30DC1803 is a fully integrated, non-synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

6.2.1 Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current remains above zero amps (see Figure 2). When the V_{FB} falls below the V_{REF}, the HS-FET turns on for a fixed duration controlled by the one-shot timer. Once the HS-FET switches off, the external free-wheeling diode carries the current.

In CCM, the switching frequency remains relatively stable, a behavior known as pulse-width modulation (PWM) mode.

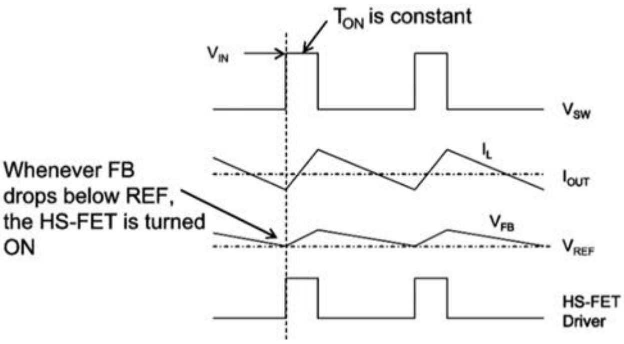


Figure 2. Heavy-Load Operation

6.2.2 Light-Load Operation

As the load decreases, the inductor current also drops. When the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load behavior is illustrated in Figure 3. When theVFB falls below the V_{REF}, the HS-FET turns on for a fixed duration determined by the one-shot timer. After the HS-FET turns off, the free-wheeling diode activates until the inductor current hits zero. In DCM, V_{FB} cannot reach V_{REF} while the inductor current approaches zero. At this point, the free-wheeling diode blocks any negative current, and the IC enters a tri-state mode. The output capacitor slowly discharges to GND via the feedback resistor, significantly enhancing efficiency during light-load conditions.In light-load mode, the HS-FET activates less frequently compared to heavy-load conditions, a behavior known as skip mode.

At light or no load, the output drops very slowly, and the GD30DC1803 naturally lowers its switching frequency, thereby achieving high efficiency during light loads.

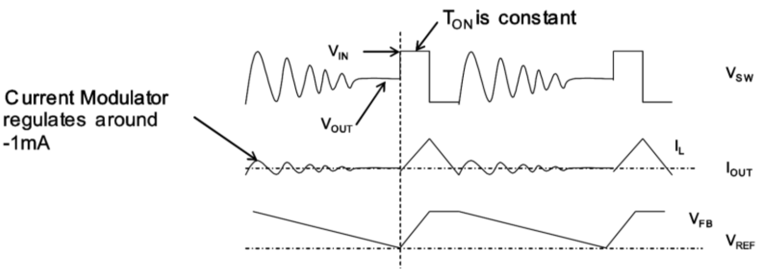


Figure 3. Light-Load Operation

As the output current rises from a light-load state, the HS-FET is activated more frequently, leading to an increase in the switching frequency. When the modulation time reduces to zero, the output current reaches the critical level.

The critical output current can be calculated using the equation provided below.

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device switches to PWM mode once the output current surpasses the critical level. Afterward, the switching frequency remains relatively stable across the output current range.

6.2.3 Enable (EN) Control

The GD30DC1801 includes a dedicated enable control pin with positive logic. To activate the regulator, apply a voltage above 1.2V (typical) to the EN pin, and to disable it, set the EN pin voltage below 0.95V (typical).

The EN pin includes an internal 4μA pull-up current source, enabling the GD30DC1801 to automatically start up when the EN pin is left floating.

To shut down the regulator via the EN pin, a pull-down current greater than 4μA is required. Once the EN pin is pulled low, the internal pull-up current reduces to 1μA, minimizing the shutdown current.

By using two external resistor dividers, the start and stop voltages of the system can be easily optimized via the EN pin.

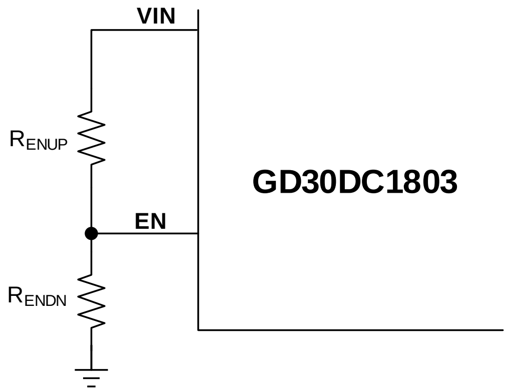


Figure 4. EN divider for adjustable UVLO

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 0.95 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (3)$$

6.2.4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The GD30DC1803 UVLO comparator monitors the input voltage. The UVLO rising threshold is about 4.3V, while its falling threshold is consistently 4.05V.

6.2.5 Internal Soft Start (SS)

The soft-start (SS) function prevents output voltage overshoot during start-up. When the chip powers on, the internal circuit generates a soft-start voltage (V_{SS}) that gradually increases from 0V to 1V. While V_{SS} remains below V_{REF}, V_{SS} replaces V_{REF} as the reference for the error amplifier. Once V_{SS} surpasses V_{REF}, the error amplifier switches back to using V_{REF}. The soft-start duration is internally set to 1.8ms.

6.2.6 Switching Frequency Set

The SET PIN can determine the switching frequency. GD30DC1803 has three options for switching frequency: 150kHz, 240kHz and 460kHz. Selecting the switching frequency can be done by choosing the resistance value of the resistor connected between SET and GND. See below table:

Table 1. Switching frequency set resistor selection

SET	Switching Frequency
Float or Connected to EN pin	460 kHz
150 kΩ (±10%) to GND	240 kHz
75 kΩ (±10%) to GND	150 kHz

6.2.7 Current Limit and Short Protection

The GD30DC1803 has a peak current limit and a special valley current. During HS-FET on, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after blanking time, the HS-FET would be turn off. Due to the peak current limit's blanking time, the inductor current might runaway when output shorts to ground for a non-sync buck. The special valley current limit in GD30DC1803 can prevent this. When HS-FET is off and the inductor current is larger than the valley current limit, the HS-FET keeps off until the output current drops below the valley current limit threshold. It's a hiccup type protection.

When the output is short to ground, GD30DC1803 will fold back the switching frequency automatically to prevent the current from runaway. It will make the system more reliable.

6.2.8 Thermal Shutdown

The thermal shutdown feature protects the chip from excessive temperatures. If the silicon die temperature exceeds 160°C, the chip automatically powers down. It reactivates once the temperature drops below the lower threshold, typically 140°C.

7 Application Information

7.1 Typical Application Circuit

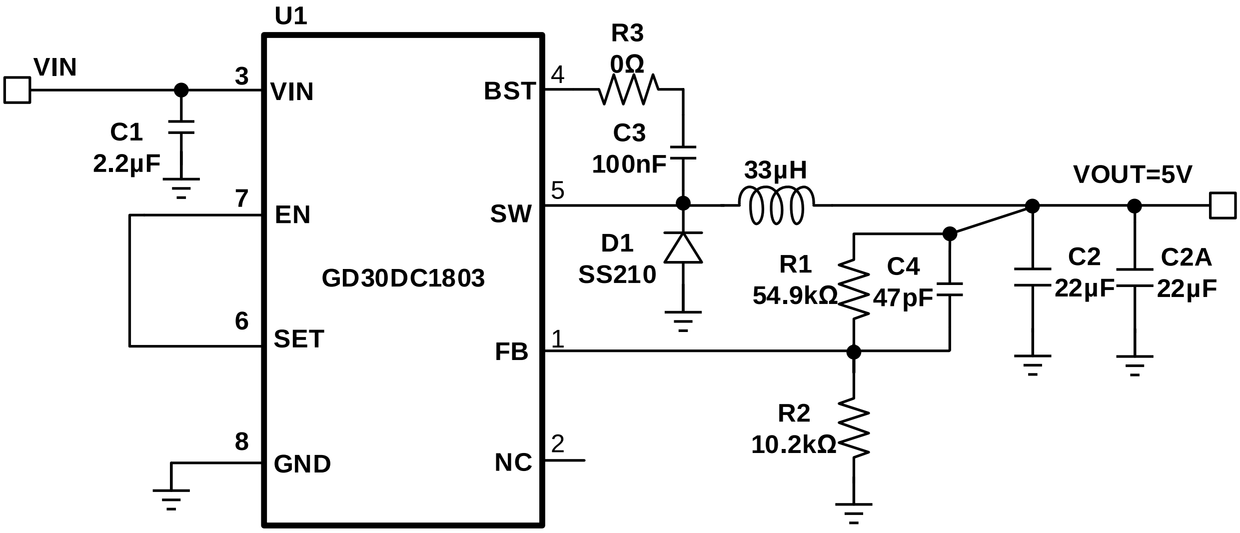


Figure 5. V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A, Fsw=460kHz[1]

1. Connect SET pin to EN pin or keep it floating to set 460kHz switching frequency.

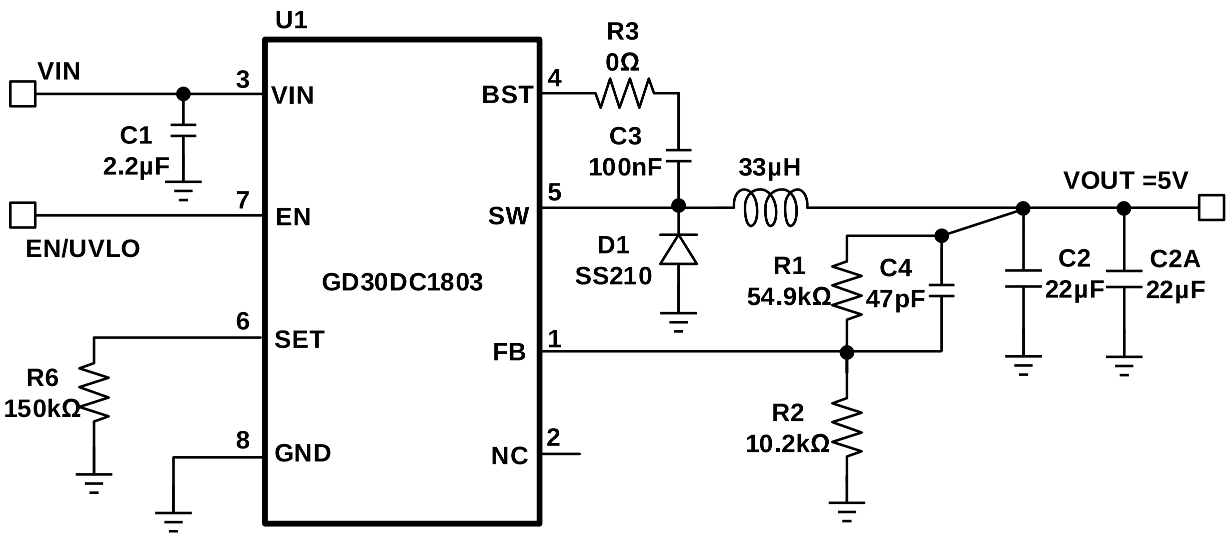


Figure 6. V_{IN}=48V, V_{OUT}=5V, I_{OUT}=2A, Fsw=240kHz

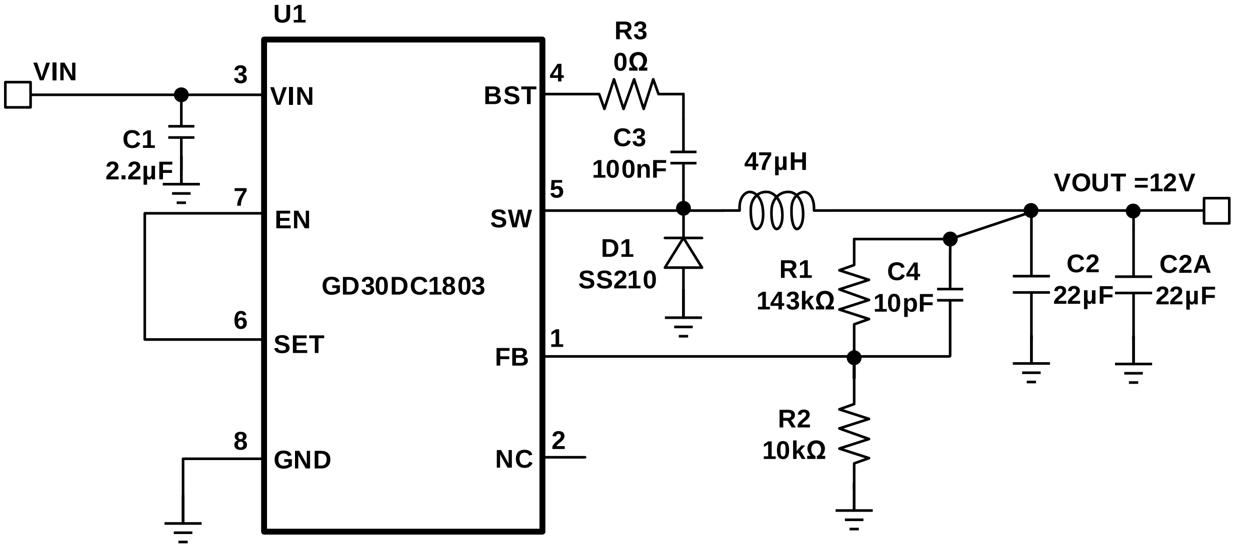


Figure 7. V_{IN}=48V, V_{OUT}=12V, I_{OUT}=1.5A, Fsw=460kHz[1]

1. Connect SET pin to EN pin or keep it floating to set 460kHz switching frequency.

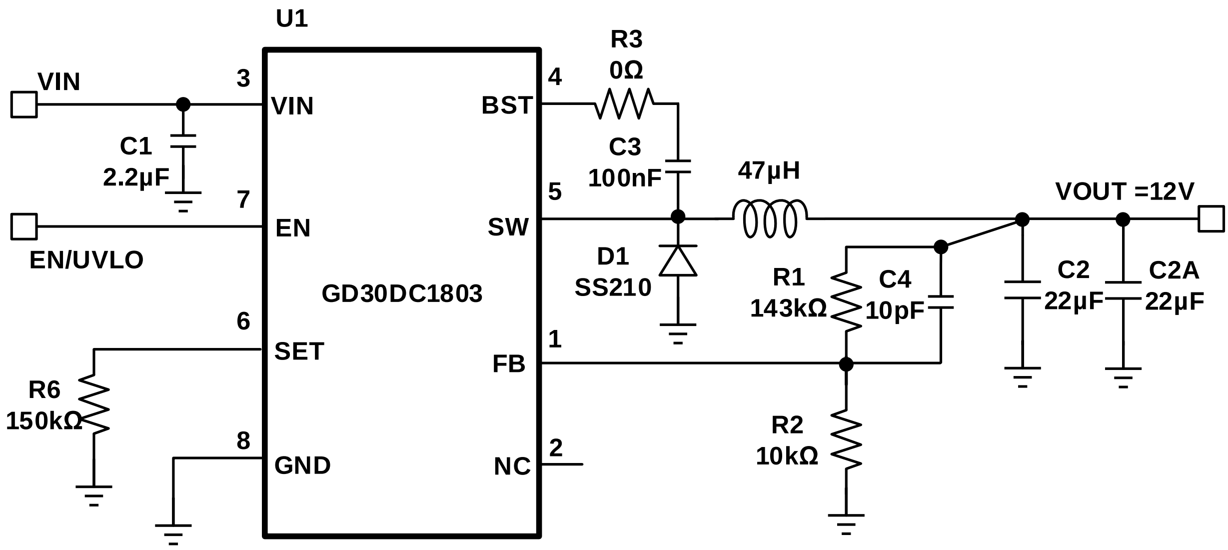


Figure 8. V_{IN}=48V, V_{OUT}=12V, I_{OUT}=1.5A, Fsw=240kHz

7.2 Detailed Design Description

7.2.1 Setting the Output Voltage

The GD30DC1803 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.78V. The feedback network is shown in Figure 9.

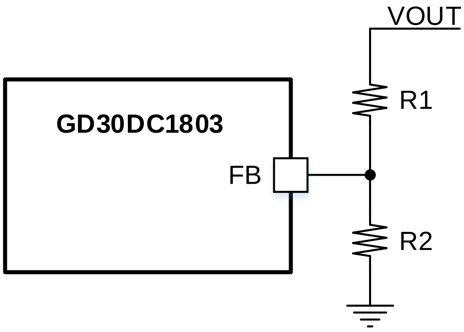


Figure 9. Feedback resistor divider

Choose R_1 and R_2 using Equation(4):

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \tag{4}$$

7.2.2 Selecting the Inductor

An inductor is essential for providing continuous current to the load while being driven by the switched input voltage. A larger inductor minimizes ripple current and reduces output voltage ripple but comes with drawbacks such as a larger physical size, higher series resistance, and lower saturation current. For most designs, the suitable inductance value can be calculated using the following Equation(5):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \tag{5}$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation(6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \tag{6}$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2. Resistor Selection for Common Output Voltages[1]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff} (pF)	L (μH)	C_{OUT} (μF)
12	143	10	10	47	2*22
5	54.9	10.2	47	33	2*22

1. For a detailed design circuit, please refer to the *Typical Application Circuit.*

7.2.3 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation(7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The GD30DC1803 can be optimized for a wide range of capacitance and ESR values.

7.3 Typical Characteristics

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 47μH, and T_A = +25°C, unless otherwise noted.

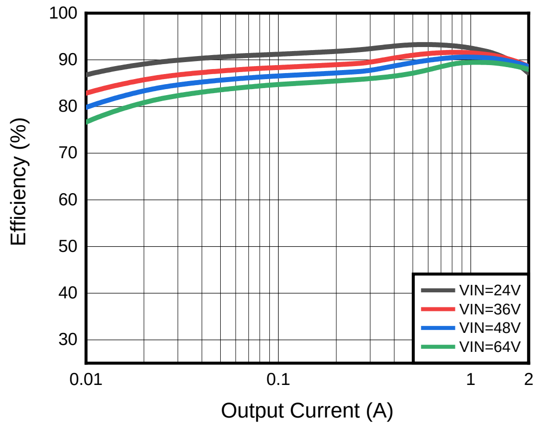


Figure 10. Efficiency vs. Load Current (F_{SW}=240kHz, L=47μH, DCR=85mΩ)

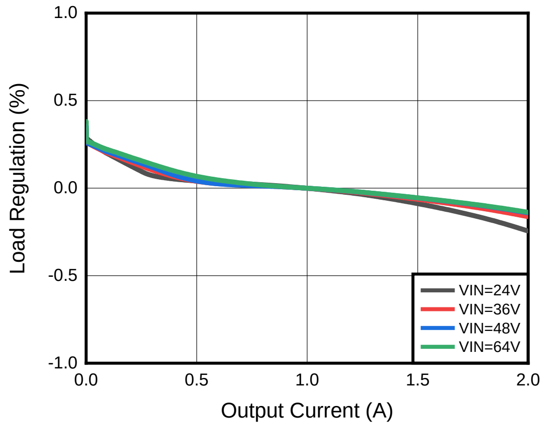


Figure 11. Load Regulation (F_{SW}=240kHz, L=47μH, DCR=85mΩ)

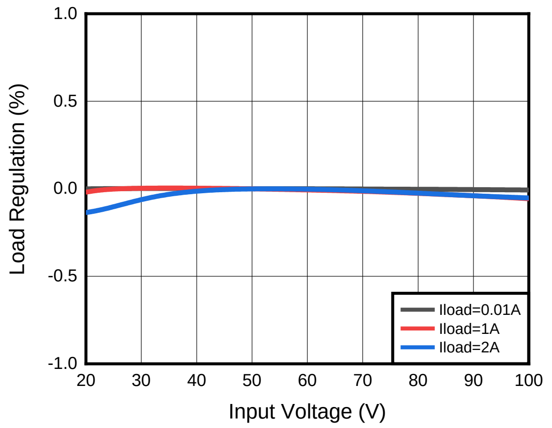


Figure 12. Line Regulation (F_{SW}=240kHz, L=47μH, DCR=85mΩ)

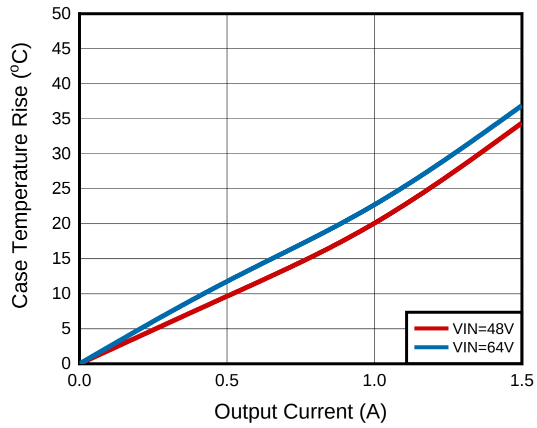


Figure 13. Thermal Rise (F_{SW}=240kHz, No air flow)

Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 5V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 33μH, and T_A = +25°C, unless otherwise noted.

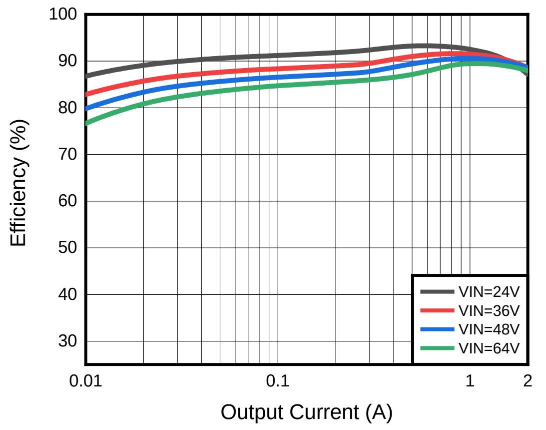


Figure 14. Efficiency vs. Load Current (Fsw=240kHz, DCR=68.4mΩ)

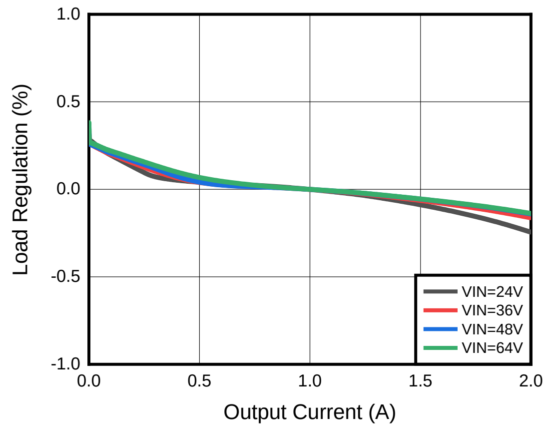


Figure 15. Load Regulation (Fsw=240kHz, DCR=68.4mΩ)

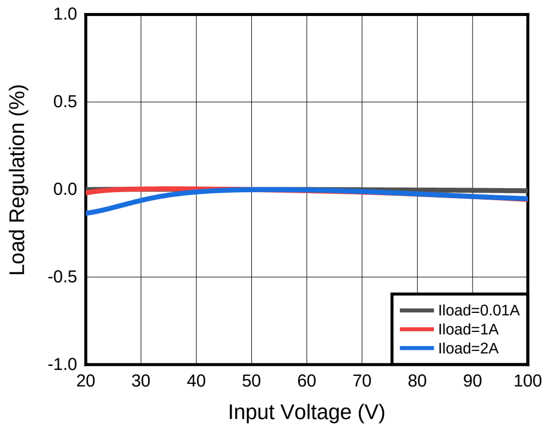


Figure 16. Line Regulation (Fsw=240kHz, DCR=68.4mΩ)

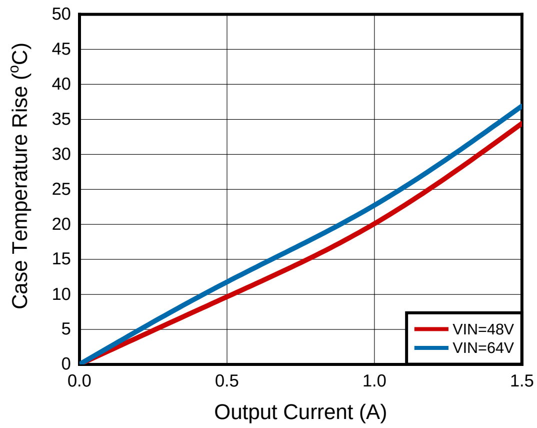


Figure 17. Thermal Rise (Fsw=240kHz, No air flow)

Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 47μH, F_{SW}=240kHz, and T_A = +25°C, unless otherwise noted.

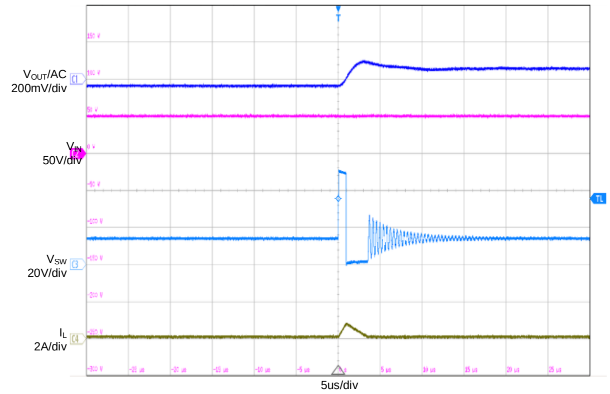


Figure 18. Output Voltage Ripple (I_{OUT} = 0A)

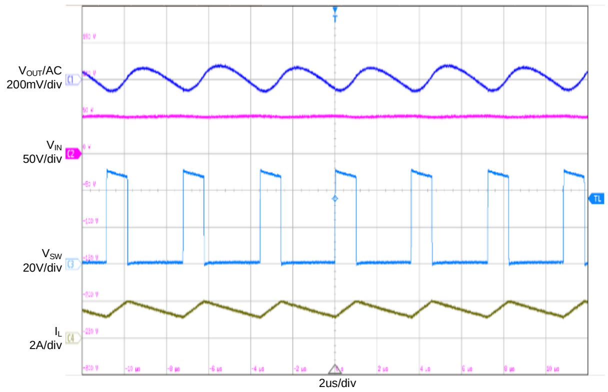


Figure 19. Output Voltage Ripple (I_{OUT} = 1.5A)

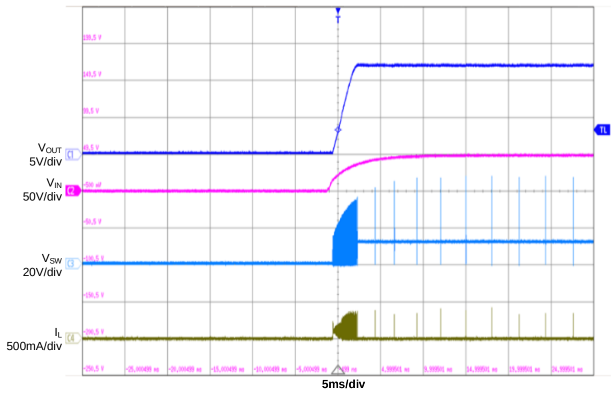


Figure 20. Startup through V_{IN} (I_{OUT} = 0A)

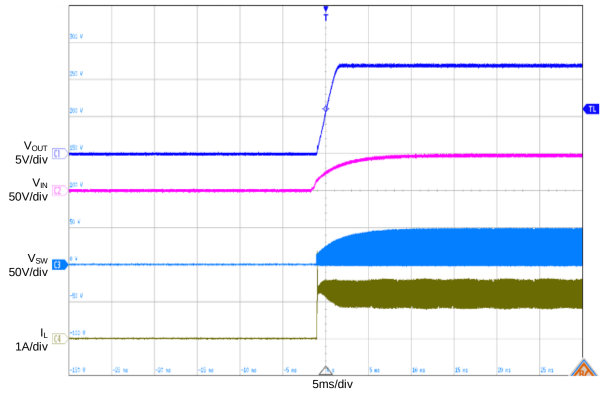


Figure 21. Startup through V_{IN} (I_{OUT} = 1.5A)

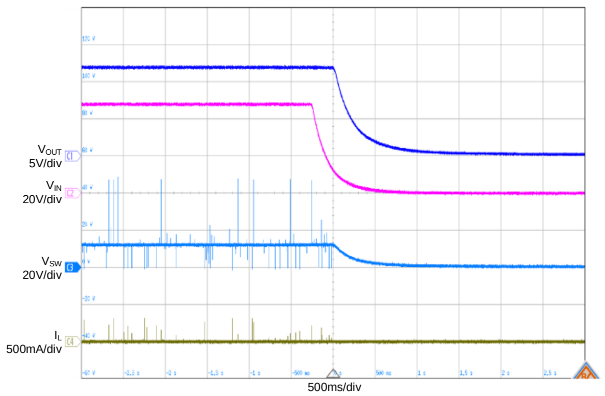


Figure 22. Shutdown through V_{IN} (I_{OUT} = 0A)

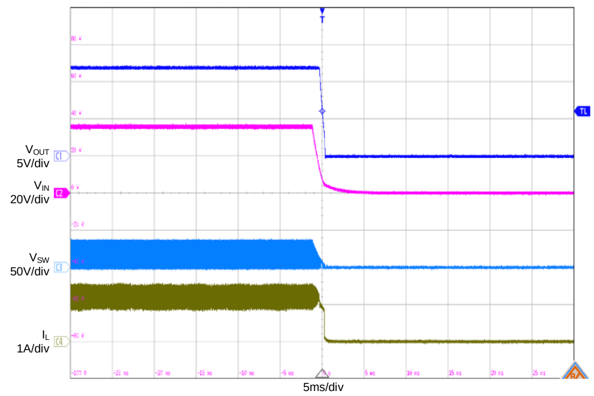


Figure 23. Shutdown through V_{IN} (I_{OUT} = 1.5A)

Typical Performance Characteristic (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2µF, C_{OUT} = 2x22µF, L1 = 47µH, F_{SW}=240kHz, and T_A = +25°C, unless otherwise noted.

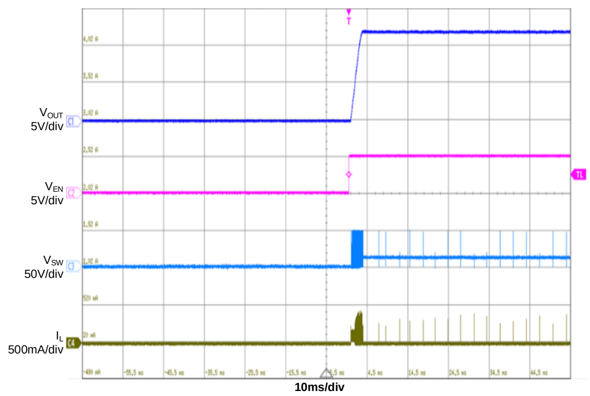


Figure 24. Startup through EN (I_{OUT} = 0A)

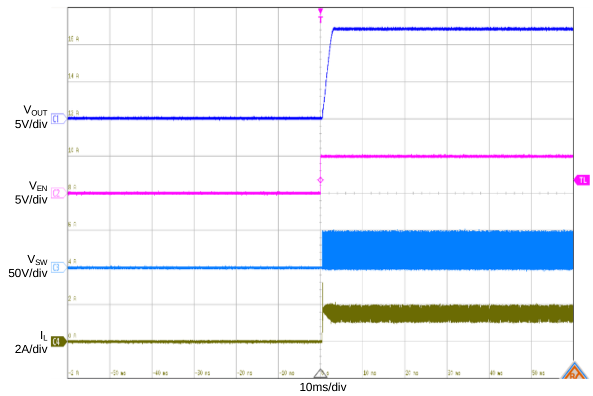


Figure 25. Startup through EN (I_{OUT} = 1.5A)

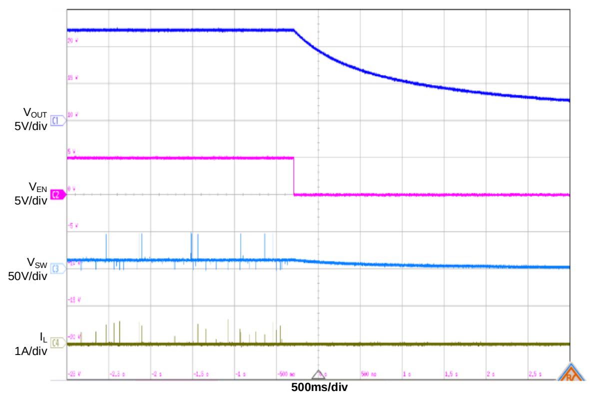


Figure 26. Shutdown through EN (I_{OUT} = 0A)

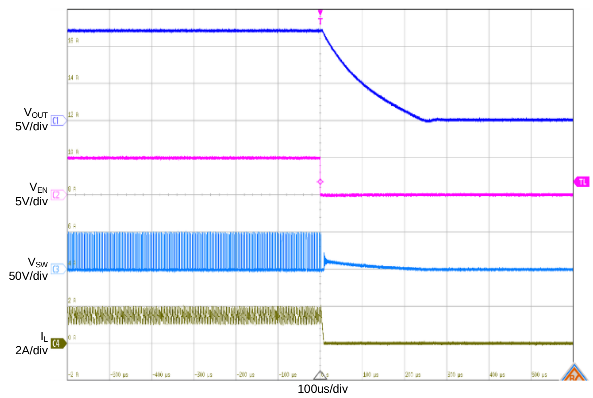


Figure 27. Shutdown through EN (I_{OUT} = 1.5A)

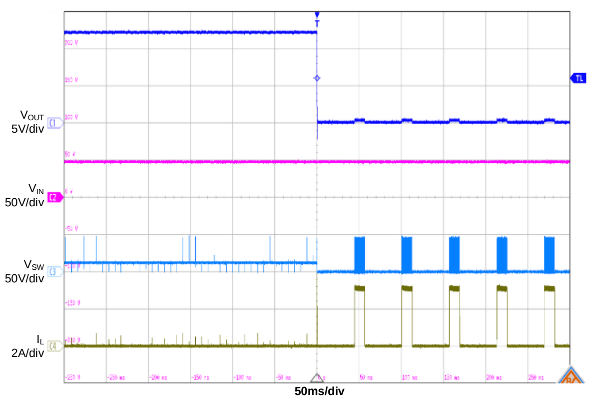


Figure 28. SCP Entry (I_{OUT} = 0A)

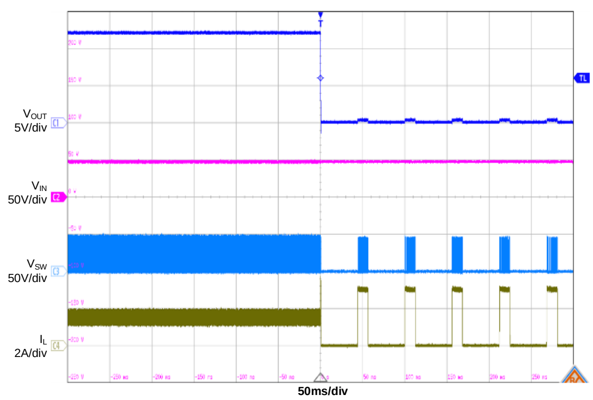


Figure 29. SCP Entry (I_{OUT} = 1.5A)

Typical Performance Characteristic (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 47μH, F_{SW}=240kHz, and T_A = +25°C, unless otherwise noted.

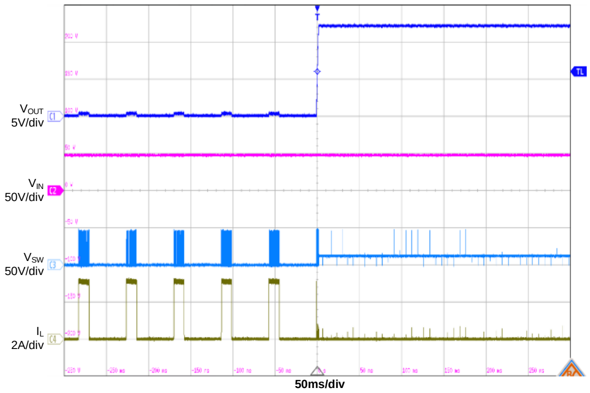


Figure 30. SCP Recovery (I_{OUT} = 0A)

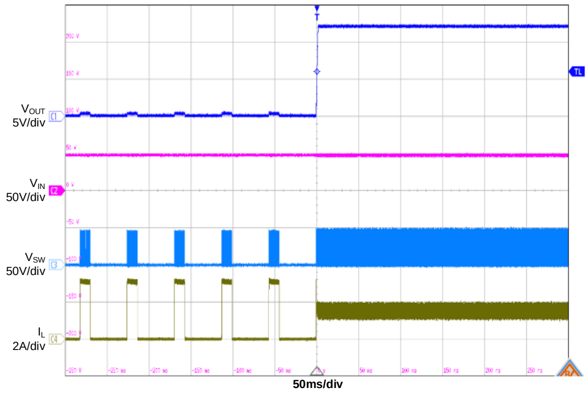


Figure 31. SCP Recovery (I_{OUT} = 1.5A)

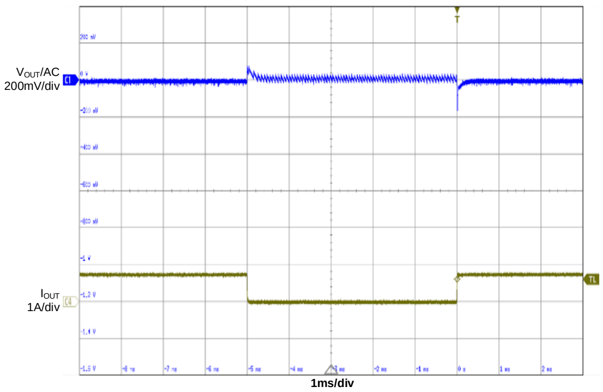


Figure 32. Load Transient (V_{OUT}=5V, L=47μH, I_{OUT} = 0.01A to 0.75A, 3A/us slew rate)

8 Layout Guidelines and Example

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

1) Place the input capacitor as close to VIN and GND as possible.
2) Place the external feedback resistors as close to FB as possible.
3) Keep the switching node (such as SW, BST) far away from the feedback network.
4) Add a grid of thermal vias under the exposed pad to improve thermal conductivity.
5) Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.

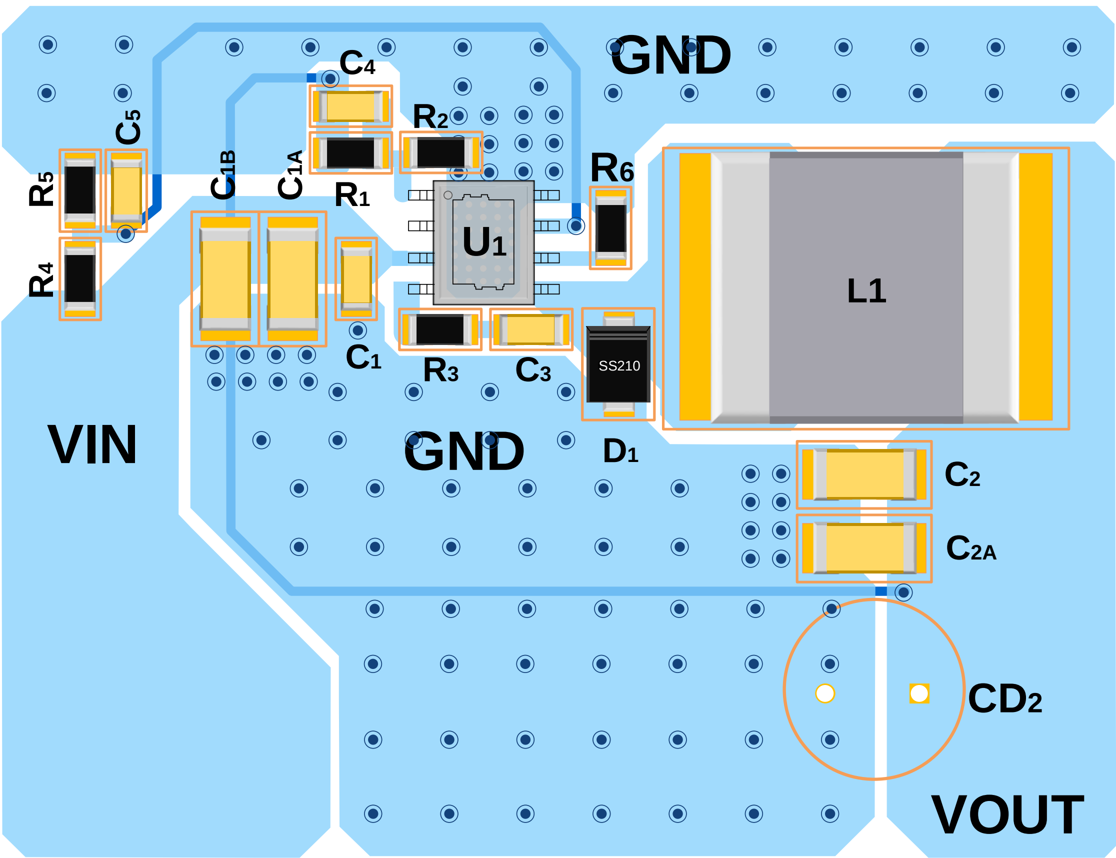
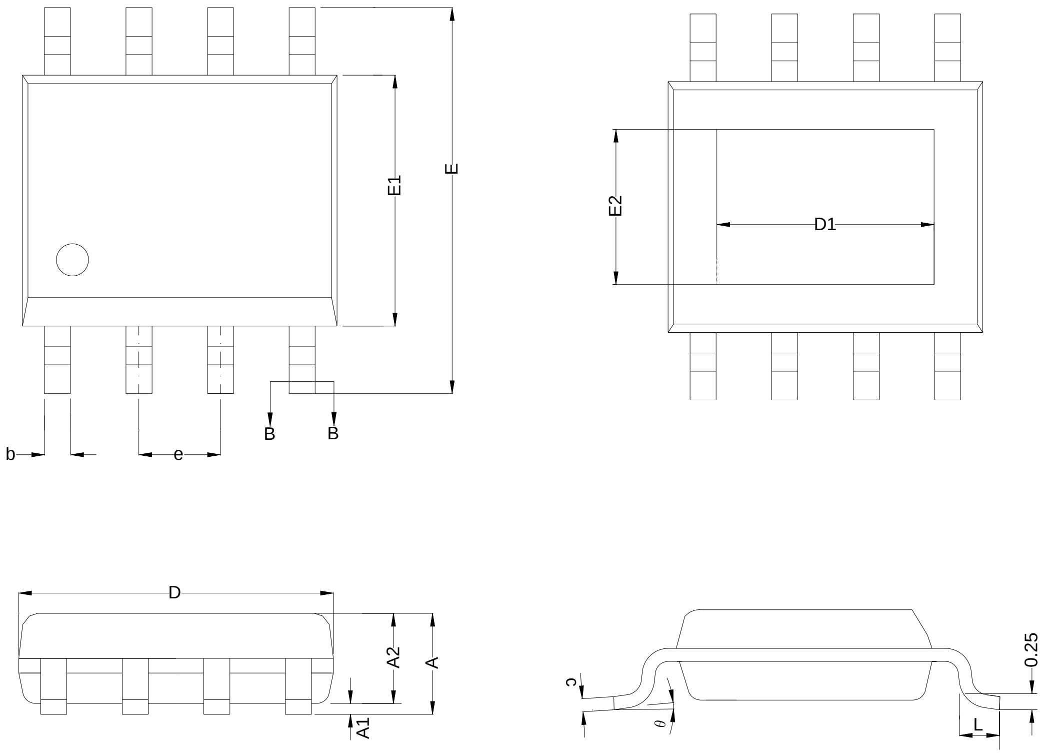


Figure 33. Typical GD30DC1803 Example Layout

9 Package Information

9.1 Outline Dimensions

ESOP8 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *ESOP8 dimensions(mm)*.

Table 3. ESOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30		1.70
b	0.33		0.51
c	0.19		0.25
D	4.80	4.90	5.00
D1	3.15		3.45
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.26		2.56
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1803WGTR-I	ESOP8	Green	Tape & Reel	4000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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