High Efficiency High Voltage 3A Step Down Converter

1 Features

- Input Voltage Range: 4.5V to 36V
- Constant Output Current: 3A
- Low R_{DS_ON} 120mΩ / 80mΩ (High/Low-side)
- Quiescent Current: 150μA
- Constant On Time Control for Fast Loop Response
- 520KHz Switching Frequency
- Support Up to 98% Large Duty Cycle
- Internal Soft Start
- 0.8V Reference Voltage
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, FB Open Short Protection, Over Temperature Protection
- Available in an ESOP8 Package

2 Applications

- Security Cameras
- Home Appliance and Whitegoods
- Multi-functional Printer
- Automotive
- Industrial Control

3 Description

The GD30DC1502 is a high efficiency synchronous step-down switch-mode converter. Which integrated low on resistance high-side and low-side power MOSFETs. The device operates from an input voltage from 4.5V up to 36V. The GD30DC1502 can deliver 3A of output current efficiently with constant on time (COT) control for fast loop response.

The GD30DC1502 achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

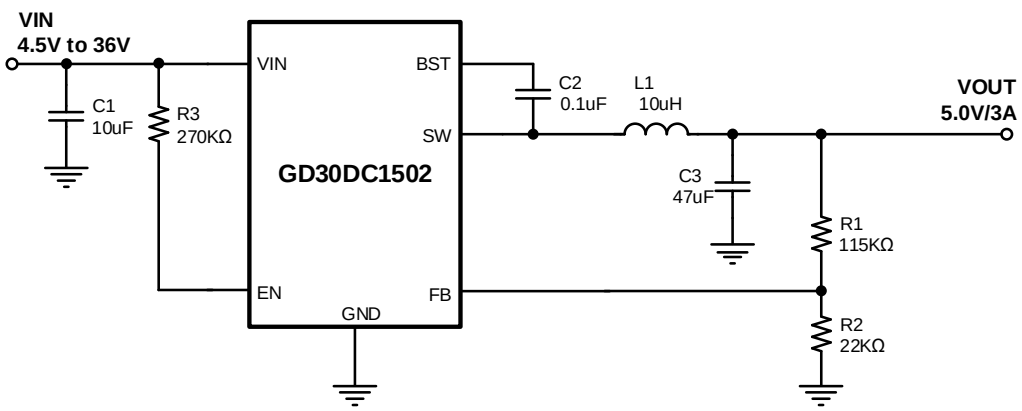
The GD30DC1502 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open short protection and thermal shutdown in case of excessive power dissipation. The GD30DC1502 is available in a space-saving ESOP8 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1502	ESOP8	4.90 mm x 3.90 mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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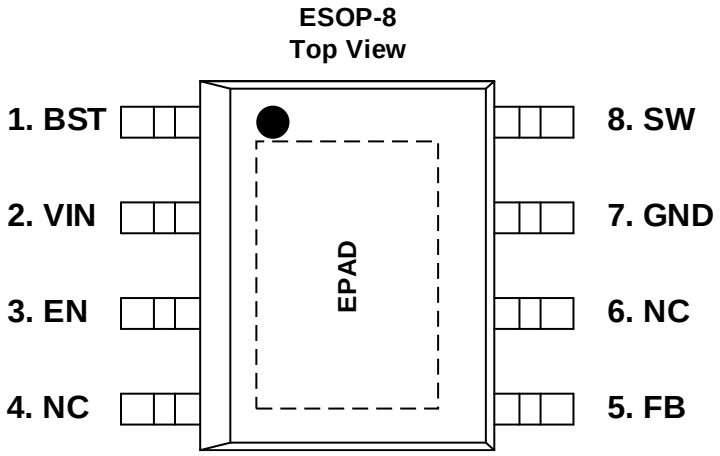
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	ESOP8		
BST	1	O	**Bootstrap**. A capacitor connection for high-side FET driver. Connect a high-quality, 0.1uF ceramic capacitor from this pin to the SW pin.
VIN	2	P	**Power supply voltage**. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
EN	3	I	**Enable**. Drive EN Pin High to enable IC, otherwise float or pull down EN to disable IC. EN pin Can be tied to VIN by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
NC	4,6		**No connection**. No connection pin for GD30DC1502.
FB	5	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
GND	7	G	**Power ground**.
SW	8	P	**Switch output**. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.

1. I = input, O = Output, P = power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage	−0.3	38	V
V_{SW}	Switching node voltage	−0.7 (−5V in 10ns)	V_{IN} + 0.7	V
I_{EN}	Input current to EN pin		100	μA
V_{BST}	Bootstrap pin voltage to V_{SW}	−0.3	6	V
I_{EN}	Max Input current to EN pin		100	μA
All Other Pins		−0.3	6	V
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−55	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.5		36	V
V_{OUT}	Output voltage	0.8		V_{IN} x D_{MAX} or V_{OUT}<18V	V
I_{OUT}	Output current	0		3	A
V_{BST}	Bootstrap pin voltage to V_{SW}	4		5	V

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±1500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	ESOP8	48	°C/W
Θ_{JC}	Junction to case (top) thermal resistance	ESOP8	52	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 12V, V_{EN}=2V, typical value is tested at T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	VIN operation input voltage		4.5		36	V
V_{UVLO_FALL}	Under voltage lockout		3.8	3.95	4.05	V
V_{UVLO_RISE}	Under voltage lockout		4.1	4.2	4.3	
V_{UVLO_HYS}	Under voltage lockout hysteresis			250		mV
I_Q	Quiescent current	No load, V_{FB} = 0.83V, no switching		150		μA
I_{SHDN}	Shutdown current	V_{EN} < 0.3V, V_{IN} = 24V		1	3	μA
ENABLE						
V_{EN_RISE}	Rising		1.1	1.2	1.3	V
V_{EN_FALL}	Falling		0.8	0.9	1.0	V
$V_{EN\text{-}HYS}$	Hysteresis			300		mV
R_{EN}	Enable input resistor.			1500		kΩ
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	T_J = 25°C	784	800	816	mV
V_{FB_UV}	Feedback under voltage threshold			300		mV
I_{FB}	Feedback leakage current	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
INTEGRATED POWER MOSFETS						
$R_{DS(on)}$	High-side FET on resistance	V_{BST} − V_{SW} = 5V		120		mΩ
	Low-side FET on resistance	V_{IN} = 12V		80		mΩ
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 12V			1	μA
CURRENT LIMIT						
I_{LIM_LS}	Low-side valley current limit	V_{OUT}=0V		3.5		A
I_{ZCD}	Zero-Current Detection					mA
SWITCHING						
T_{ONMIN}[1]	Minimum on time			80		ns
T_{OFFMIN}[1]	Minimum off time			120		ns
D_{MAX}[1]	Max duty cycle			98		%
Tss	Soft-Start time	V_{FB} from 0% to 100%		2.4		ms
F_{SW}	Oscillator frequency			520		KHz
THERMAL SHUTDOWM						
T_{TSD}[1]	Thermal shutdown temperature			150		°C
T_{HYS}[1]	Thermal shutdown hysteresis			20		°C

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 10μF, C_{OUT} = 44μF, L1 = 10μH, and T_A = 25°C, unless otherwise noted.

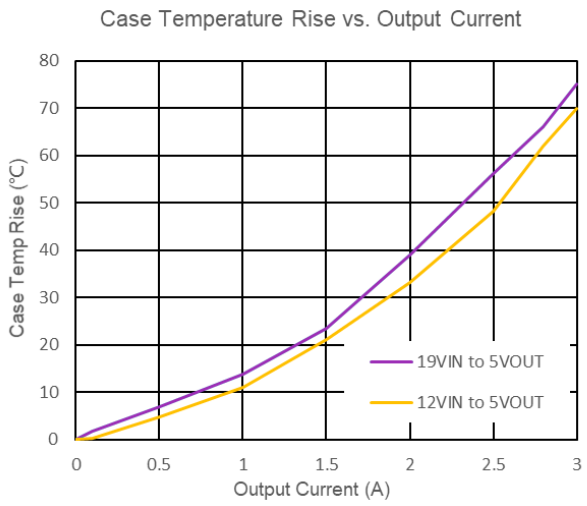


Figure 1. Temperature Rise

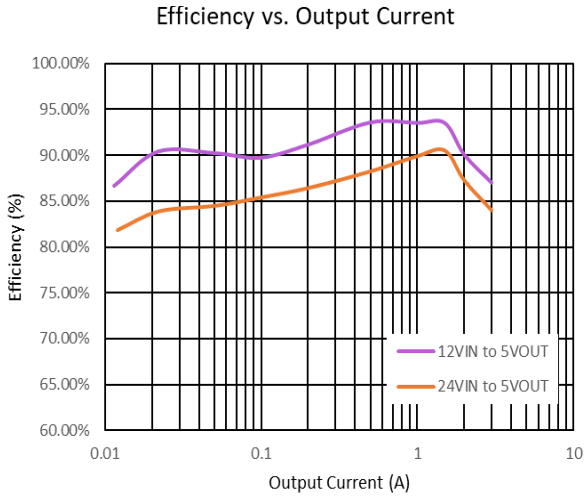


Figure 2. Output Efficiency

6 Functional Description

6.1 Block Diagram

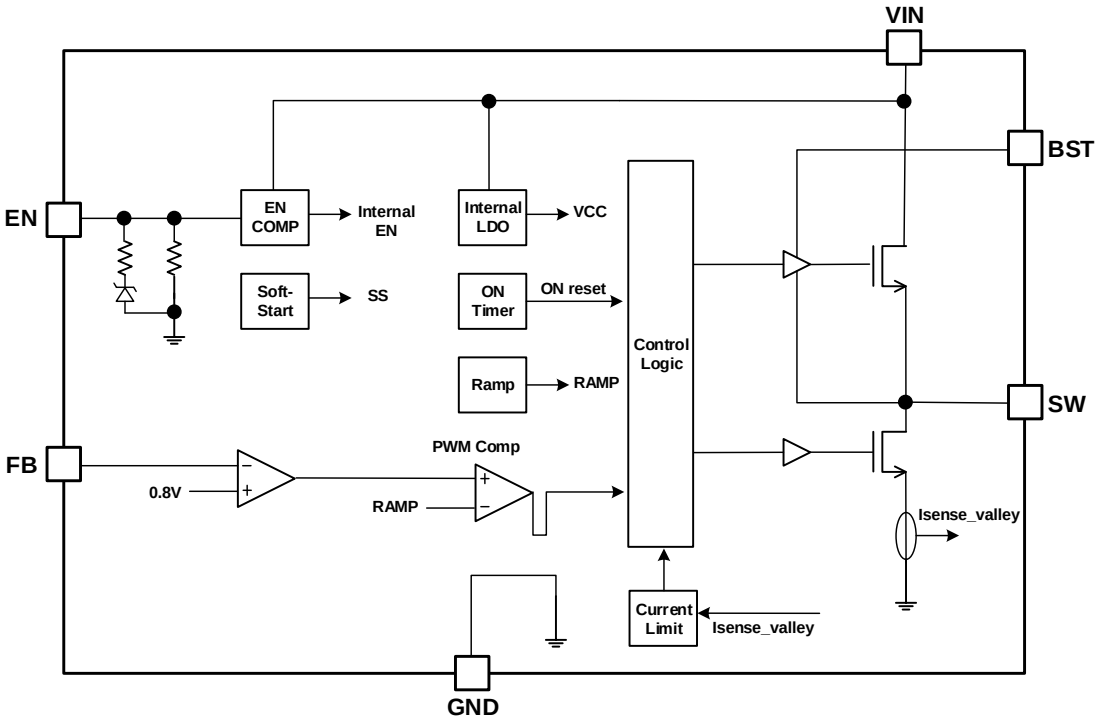


Figure 3. GD30DC1502 Functional Block Diagram

6.2 Operation

The GD30DC1502 is a synchronous switching step-down converter. The adaptive on-time is so controlled by the input/output voltage that the IC operates at relative constant frequency, typically 520kHz. It is capable of delivering up to 3A for VIN between 4.5V and 36V. The output voltage can be as low as 0.8V.

6.2.1 Pulse-Width Modulation (PWM) Control

The GD30DC1502 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (VREF), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low- side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. To avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

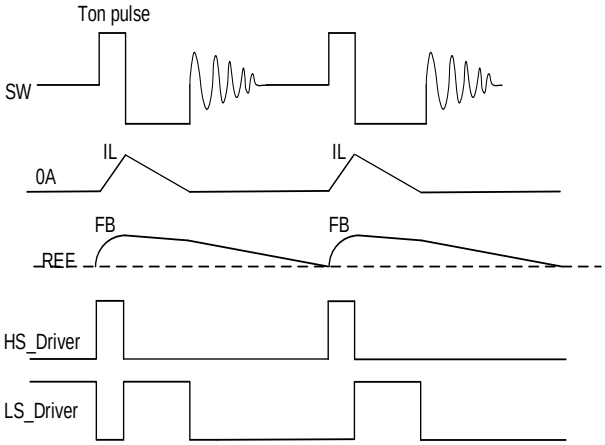


Figure 4. PFM Operation

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous- conduction-mode (DCM).

When the GD30DC1502 works in pulse-frequency modulation (PFM) mode during light-load operation, the GD30DC1502 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side will be off the GD30DC1502 enters Hi-zi state. The output capacitors discharge slowly to GND through R1 and R2. When V_{FB} drops below the reference voltage, the HS-FET is turned on again. This operation improves device efficiency greatly when the output current is low.

6.2.2 Soft Startup

After enabling the device, internal soft-start circuitry monotonically ramps up the output voltage which reaches nominal output voltage during a soft-start time of 2.4ms (typical). This avoids excessive inrush current and creates a smooth output voltage rise slope.

6.2.3 Pre-Bias startup

The GD30DC1502 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

6.2.4 Under Voltage Lockout

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The GD30DC1502 UVLO comparator monitors the input voltage. The UVLO rising threshold is 4.2V(typical), while its falling threshold is consistently 3.95V.

6.2.5 Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The GD30DC1502 has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the LS limit compactor active. The device enters over current protection mode. High side will not be turned on until the valley current limit disappear. Meanwhile, the output voltage drops until V_{FB} is below the under voltage (UV) threshold. Once UV is triggered, the GD30DC1502 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

6.2.6 Large Duty Cycle Operation

When GD30DC1502 will automatically extend the On time to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The GD30DC1502 can support up to 98% maximum duty cycle.

6.2.7 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 150°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 20°C (typical), the device returns to normal operation automatically.

6.3 Device Mode Description

6.3.1 Device Enable

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 4.2V), the GD30DC1502 can be enabled by pulling EN higher than 1.2V. Leaving EN floating or pulling it down to ground disables the GD30DC1502. There is an internal 1.5MΩ resistor from EN to ground. EN is clamped internally using a 5.5V Zener diode. EN can connected to VIN directly by a resistor.

The EN Pin can connect to VIN by a pull-up resistor, but EN input current need below 100uA. For example, if V_{IN}=24V, the I_{Zener} = (24-5.5) / $R_{PULL-UP}$ < 100uA, So, $R_{PULL-UP}$ > 185KΩ.

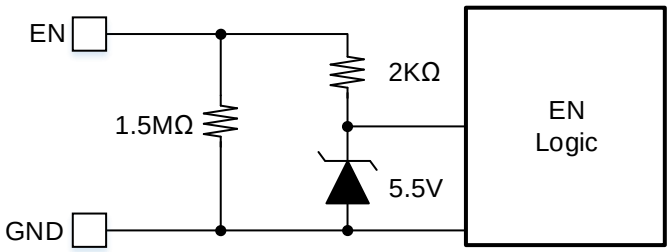


Figure 5. Zener Diode between EN and GND

7 Application Information

7.1 Typical Application Circuit

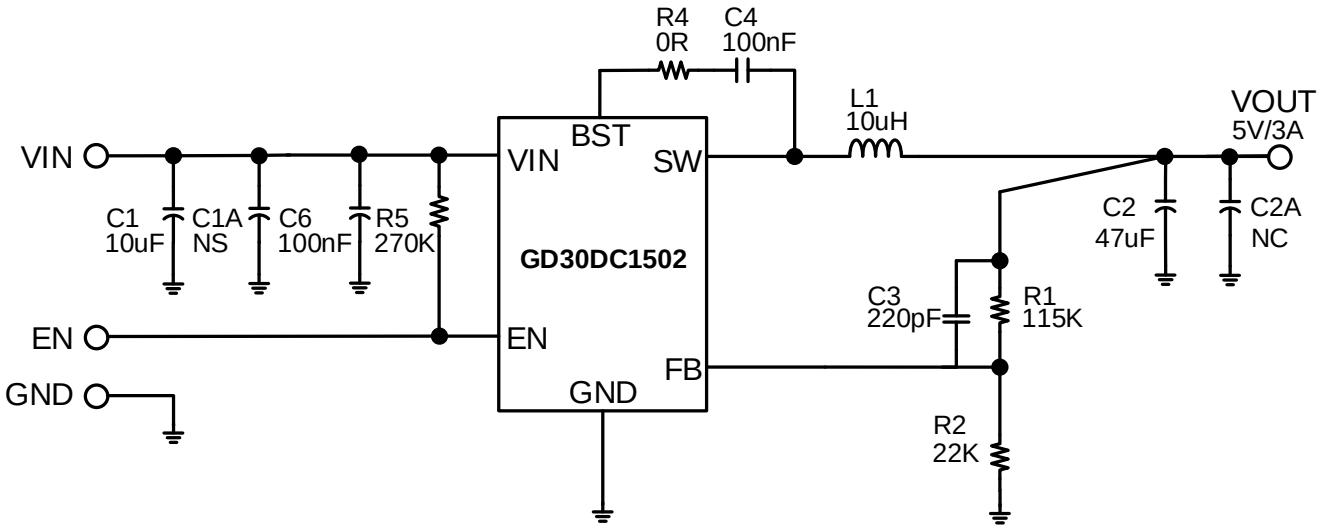


Figure 6. 5.0V, 3A Reference Design

Note: C3 is optional for better transient performance.

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	4.5V to 36V
Output Voltage	5.0V
Maximum Output Current	3A

7.3 Detailed Design Description

7.3.1 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(1). By selecting R1 and R2, the output voltage is programmed to the desired value. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It I recommended to choose a value within 2k to 100k for R2. When the output voltage is regulated, the typical voltage reference at the FB pin is 0.8V.

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

The feedback circuit is shown in Figure 7.

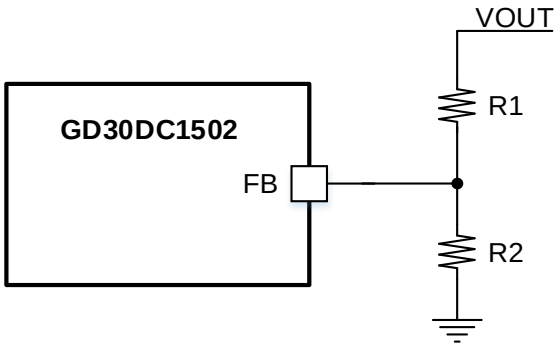


Figure 7. Feedback resistor divider

Table 2 lists the recommended parameters values for common output voltages.

Table 2. Component selection for common output voltages[1,2]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT}(μF)
5	115	22	10	47
3.3	68	21.5	8.2	47

1. The components used in these design cases do not belong to GD products, GD does not warrant its accuracy or completeness. GD's customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.
2. Refer to *Detailed Design Description* section for guidance on component selection and calculation equations.

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and hight conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(2) and Equation(3). Ensure that the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \tag{2}$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{3}$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(4). Once an inductor value is chosen, the peak inductor current is determined by Equation(3). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \tag{4}$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 22μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(5):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(6):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (6)$$

Where D is the duty cycle of converter. The worst-case condition occurs at V_{IN} = 2V_{OUT}. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor, FOSC is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (8)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The GD30DC1502 can be optimized for a wide range of capacitance and ESR values.

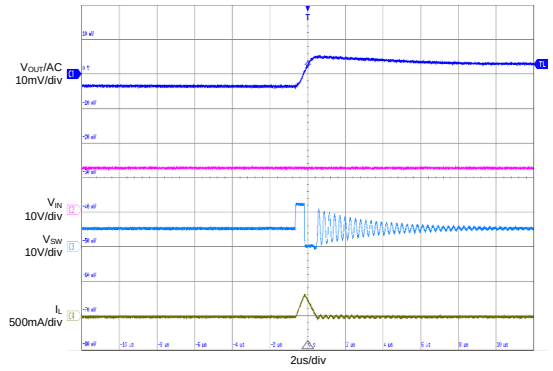
Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value COUT_max can be limited approximately by:

$$C_{OUT\_MAX} = (I_{limit_{ave}} - I_{OUT}) \times T_{SS} / V_{OUT} \quad (10)$$

Where, ILIM_AVG is the average start-up current during soft-start period, Tss is the soft-start time (2.4ms typically).

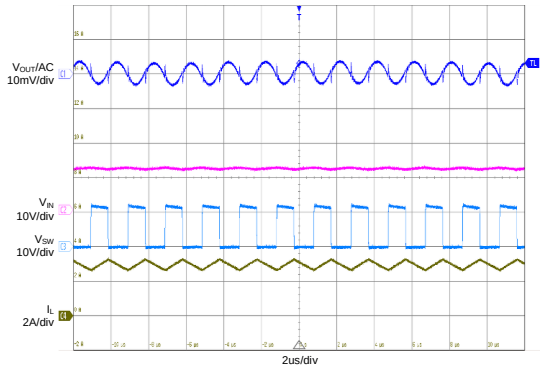
7.4 Typical Application Curves

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 10μF, C_{OUT} = 47μF, L1 = 10μH, and T_A = 25°C, unless otherwise noted.



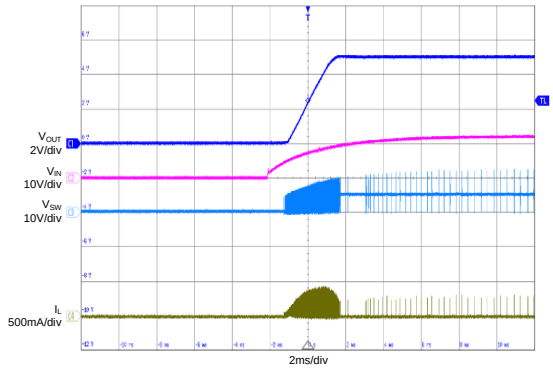
I_{OUT} = 0A

Figure 8.Output Voltage Ripple



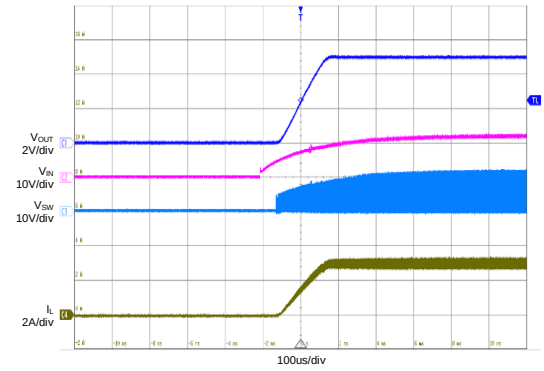
I_{OUT} = 3A

Figure 9.Output Voltage Ripple



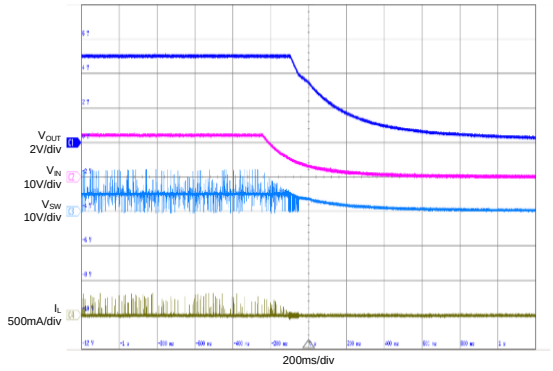
I_{OUT} = 0A

Figure 10.Start-Up through VIN



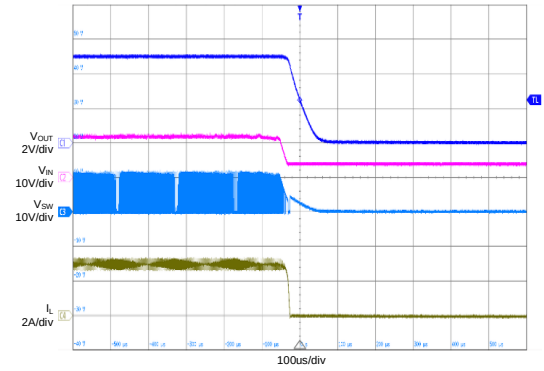
I_{OUT} = 3A

Figure 11.Start-Up through VIN



I_{OUT} = 0A

Figure 12.Shutdown through VIN

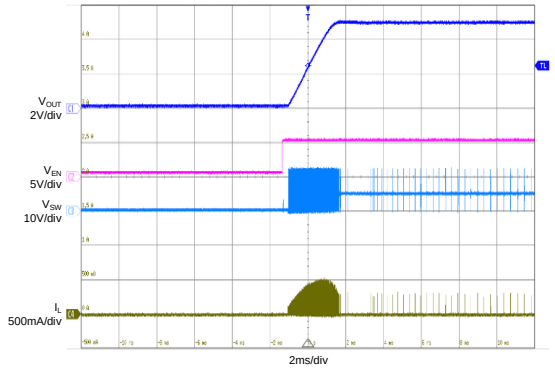


I_{OUT} = 3A

Figure 13.Shutdown through VIN

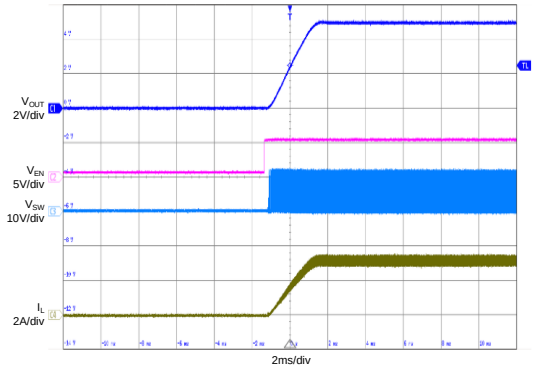
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 10μF, C_{OUT} = 47μF, L1 = 10μH, and T_A = 25°C, unless otherwise noted.



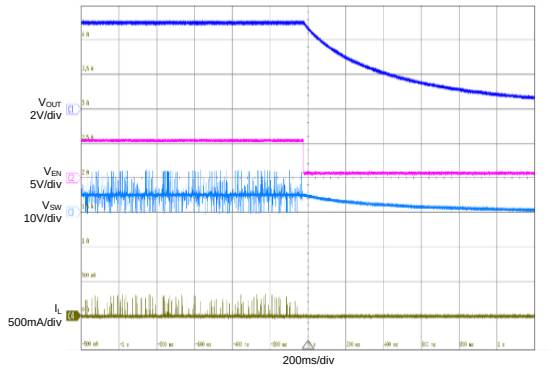
I_{OUT} = 0A

Figure 14.Start-Up through EN



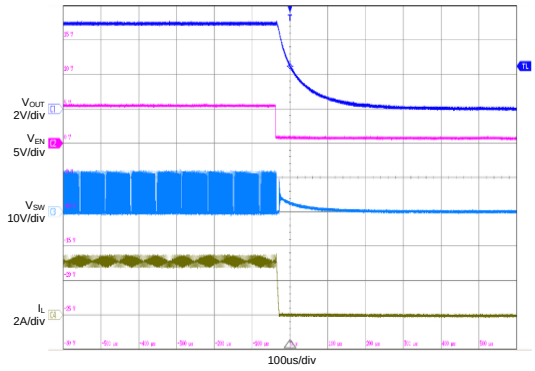
I_{OUT} = 3A

Figure 15.Start-Up through EN



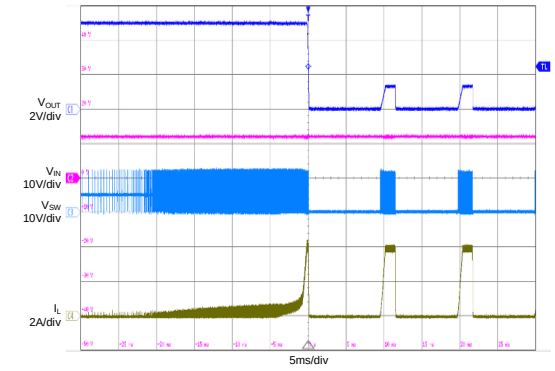
I_{OUT} = 0A

Figure 16.Shutdown through EN



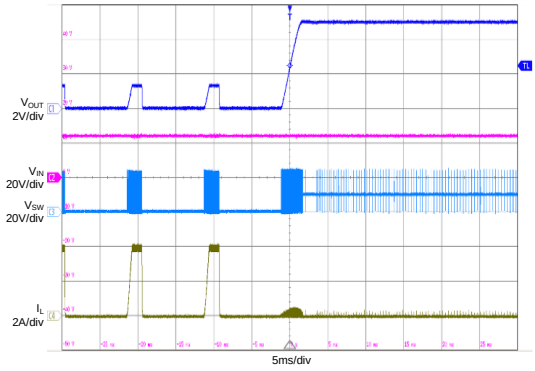
I_{OUT} = 3A

Figure 17.Shutdown through EN



I_{OUT} = 0A

Figure 18.Short Entry

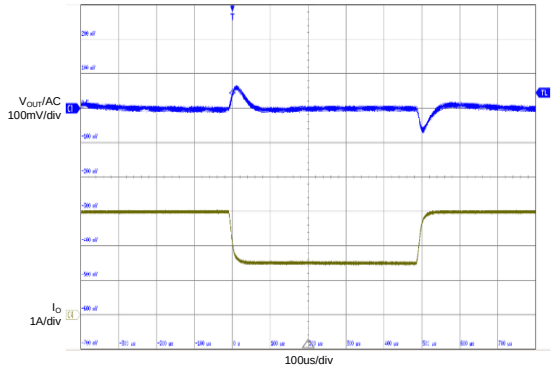


I_{OUT} = 0A

Figure 19.Short Recovery

Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 10μF, C_{OUT} = 47μF, L1 = 10μH, and T_A = 25°C, unless otherwise noted.



V_{OUT} = 3.3V, I_{OUT} = 1.5A to 3A, 2.5A/us

Figure 20.Load Transient

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

1) Place the input/output capacitor and inductor should be placed as close to IC.
2) Keep the power traces as short as possible.
3) The low side of the input and output capacitor must be connected properly to the power GND avoid a GND potential shift.
4) Place the external feedback resistors next to FB.
5) Keep the switching node SW short and away from the feedback network.

For best results, follow the layout example below.

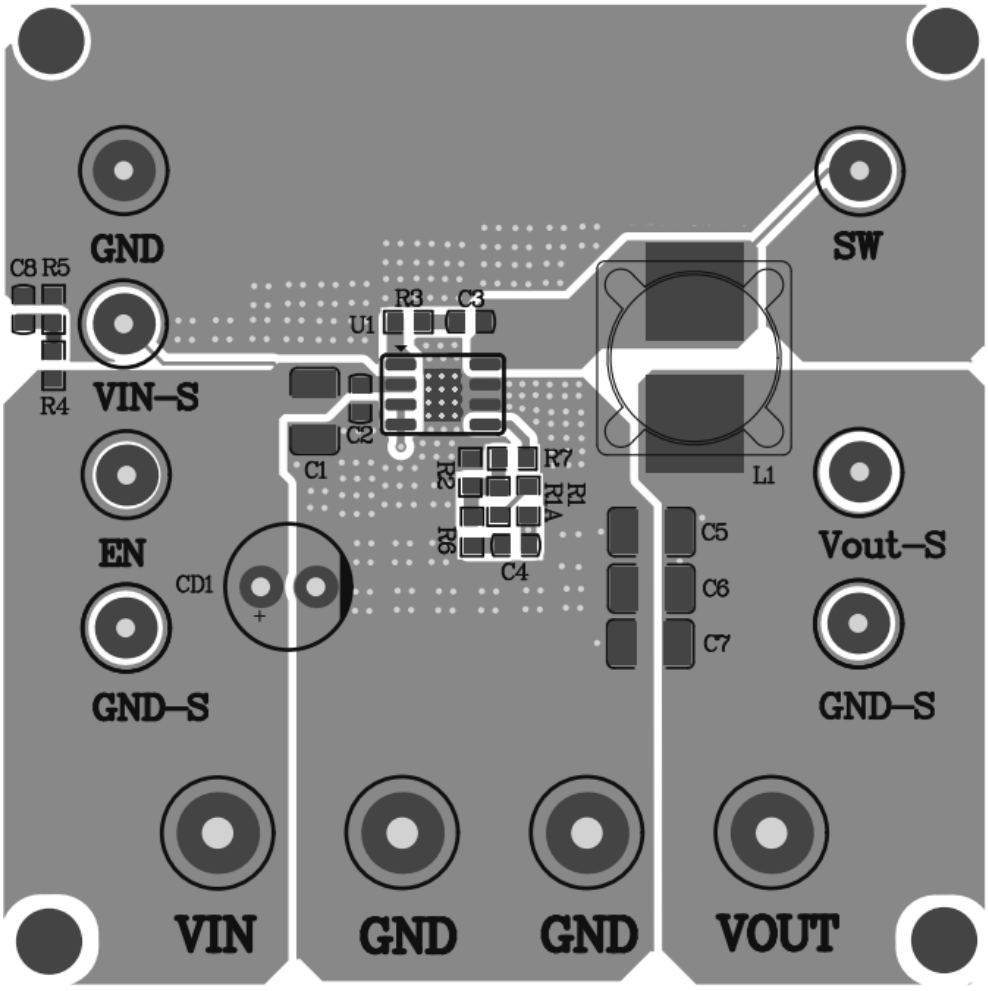
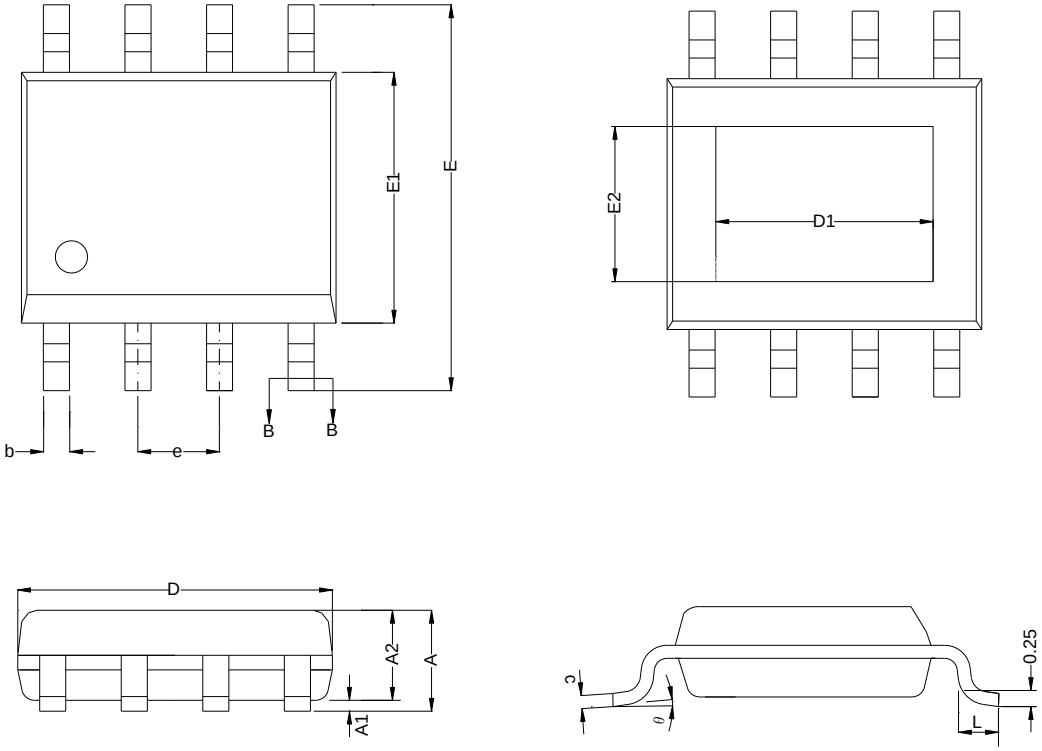


Figure 21. Typical GD30DC1502 Example Layout for Top Layer

9 Package Information

9.1 Outline Dimensions

ESOP8 Package Outline



NOTES: (continued)

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *ESOP8 dimensions(mm)*.

Table 3. ESOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30		1.70
b	0.33		0.51
c	0.19		0.25
D	4.80	4.90	5.00
D1	3.15		3.45
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.26		2.56
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1502WGTR-I	ESOP8	Green	Tape & Reel	4000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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