High Efficiency High Voltage 3A Step Down Converter

1 Features

- Input Voltage Range: 4.2V to 28V
- Constant Output Current: 3A
- Low R_{DS_ON} 90mΩ / 40mΩ (High/Low-side)
- Quiescent Current: 130μA
- Constant On Time Control for Fast Loop Response
- 600KHz Switching Frequency
- Support 100% Duty Cycle
- Internal Soft Start
- 0.6V Reference Voltage
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, Over Temperature Protection
- Available in an TSOT23-6L Package

2 Applications

- Security Cameras
- Home Appliance and Whitegoods
- Multi-functional Printer
- Automotive
- Industrial Control

3 Description

The GD30DC135A is a high efficiency synchronous step-down switch-mode converter. Which integrated low on resistance high-side and low-side power MOSFETs. The device operates from an input voltage from 4.2V up to 28V. The GD30DC135A can deliver 3A of output current efficiently with constant on time (COT) control for fast loop response.

The GD30DC135A achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

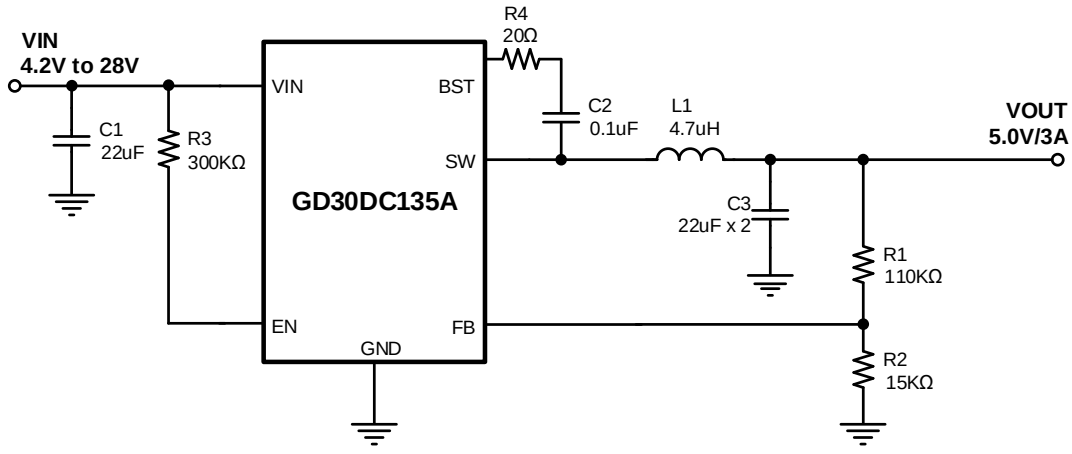
The GD30DC135A has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, FB open/short protection and thermal shutdown in case of excessive power dissipation. The GD30DC135A is available in a space-saving TSOT23-6L package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC135A	TSOT23-6L	2.92mm x 1.60mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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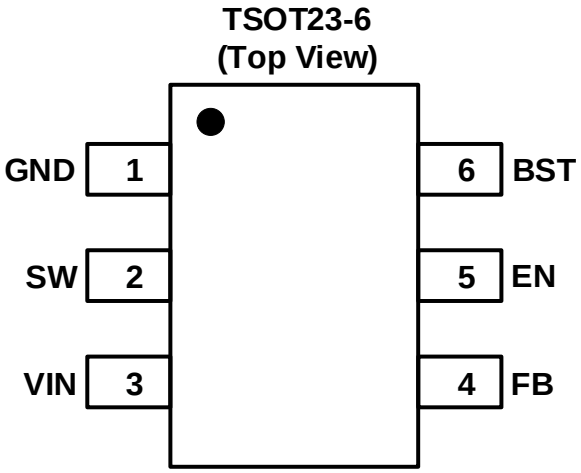
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	TSOT23-6L		
GND	1	G	**Power ground**.
SW	2	P	**Switch output**. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.
VIN	3	P	**Power supply voltage**. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
FB	4	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
EN	5	I	**Enable**. Drive EN Pin High to enable IC, otherwise float or pull down EN to disable IC. EN pin Can be tied to VIN by a resistor. Precision enable input allows adjustable UVLO by external resistor divider.
BST	6	O	**Bootstrap**. A capacitor connection for high-side FET driver. Connect a high-quality, 0.1uF ceramic capacitor from this pin to the SW pin.

1. I = input, O = Output, P = power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage	−0.3	30	V
V_{SW}	Switching node voltage	−0.7 (−5V in 10ns)	V_{IN} + 0.7	V
V_{BST}	Bootstrap pin voltage to V_{SW}	−0.3	6	V
I_{EN}	Max Input current to EN pin		100	μA
All Other Pins		−0.3	6	V
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−55	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.2		28	V
V_{OUT}	Output voltage	0.6		D_{MAX}*V_{IN}	V
I_{OUT}	Output current	0		3	A

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	TSOT23-6L	62	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	TSOT23-6L	23	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 12V, V_{EN}=2V, typical value is tested at T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{UVLO_RISE}	Under voltage lockout	VIN rising, V_{EN} = 2V		4.05		V
V_{UVLO_HYS}	Under voltage lockout hysteresis			250		mV
I_Q	Quiescent current	V_{IN}=12V,V_{EN} = 2V, V_{FB} = 0.63V, no switching		130		μA
I_{SHDN}	Shutdown current	V_{EN} = 0V, V_{IN}=12V		1	2	μA
ENABLE						
V_{EN_RISE}	Rising			1.2		V
$V_{EN\text{-}HYS}$	Hysteresis			150		mV
I_{EN}	EN input current	V_{EN} = 2V		3		μA
T_{EN_DEY}	EN turn on delay	EN rising to SW switching		300		μs
VOLTAGE REFERENCE AND SS						
V_{FB}	Feedback voltage	T_J = 25°C	594	603	612	mV
I_{FB}	Feedback leakage current	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
Tss	Soft-Start time	V_{FB} from 0% to 100%		1.2		ms
INTEGRATED POWER MOSFETS						
Fsw	Oscillator frequency			600		KHz
$R_{DS(on)}$	High-side FET on resistance	V_{BST} − V_{SW} = 5V		90		mΩ
	Low-side FET on resistance	V_{IN} = 12V		40		mΩ
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
CURRENT LIMIT						
I_{LIM_LS}	Low-side current limit			3.5		A
I_{LIM_HS}	High-side current limit			5		A
I_{NEG}	LS Negative current limit			−2.5		A
I_{ZCD}	Zero-Current Detection			50		mA
V_{OUT} OVP/UVP THRESHOLD HOLD						
V_{OVP}	Rising			120		%V_{FB}
V_{UVP}	FB UV threshold			25		%V_{FB}
T_{OFFMIN}[1]	Minimum off time			120		ns
T_{ONMIN}(1)	Minimum on time			40		ns
D_{MAX}(1)	Max duty cycle			100		%
THERMAL SHUTDOWM						
T_{TSD}[1]	Thermal shutdown temperature			160		°C
T_{HYS}[1]	Thermal shutdown hysteresis			25		°C

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 22x2μF, L1 = 4.7μH, Frequency = 600kHz, and T_A = 25°C, unless otherwise noted.

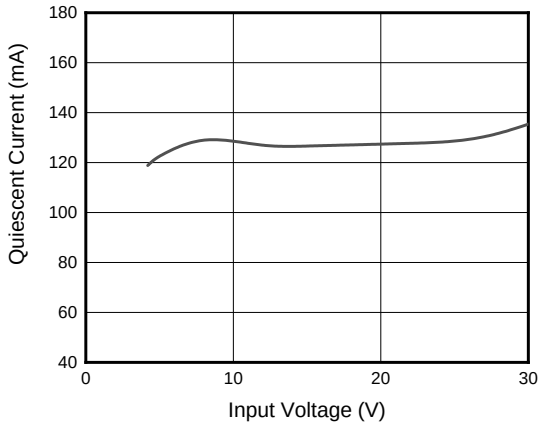


Figure 1. Quiescent Current vs. Input Voltage

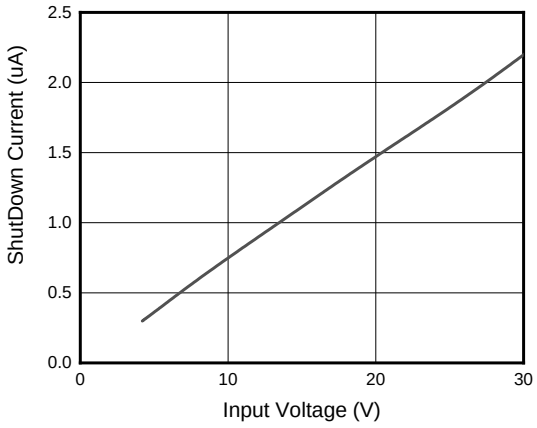


Figure 2. Shutdown Current vs. Input Voltage

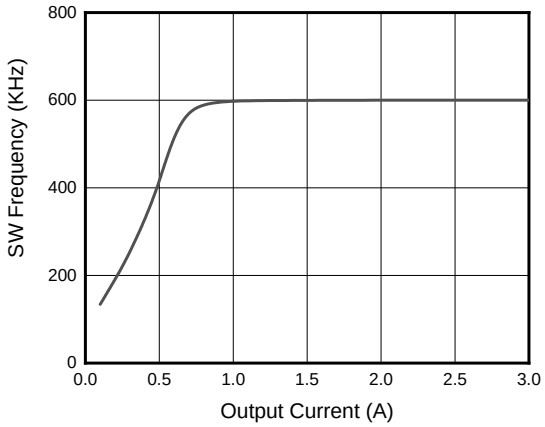


Figure 3. Frequency vs. Output Current

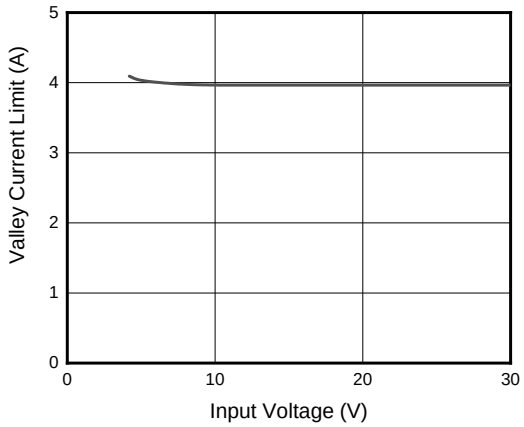


Figure 4. Valley Current Limit vs. Input Voltage

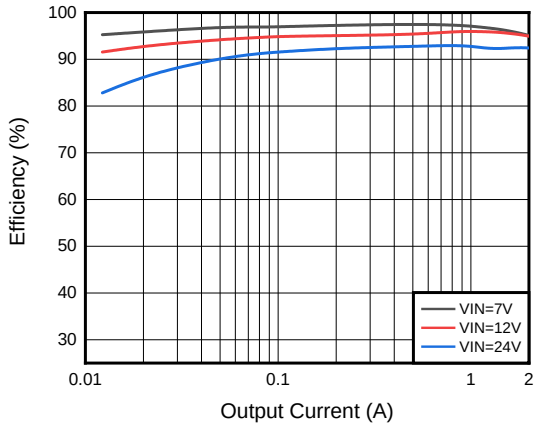


Figure 5. 5V Efficiency

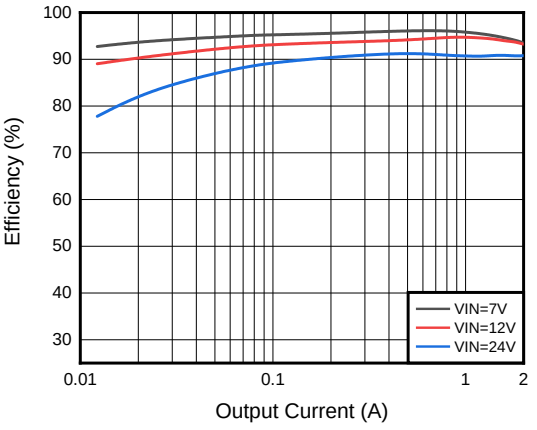


Figure 6. 3.3V Efficiency

Typical Characteristic (continued)

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22µF, C_{OUT} = 44µF, L1 = 10µH, and T_A = 25°C, unless otherwise noted.

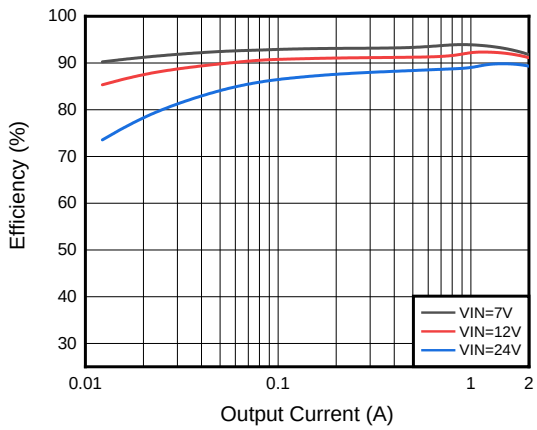


Figure 7. 2.5V Efficiency

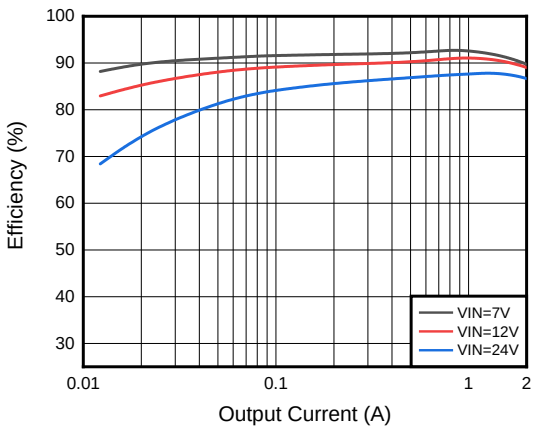


Figure 8. 1.8V Efficiency

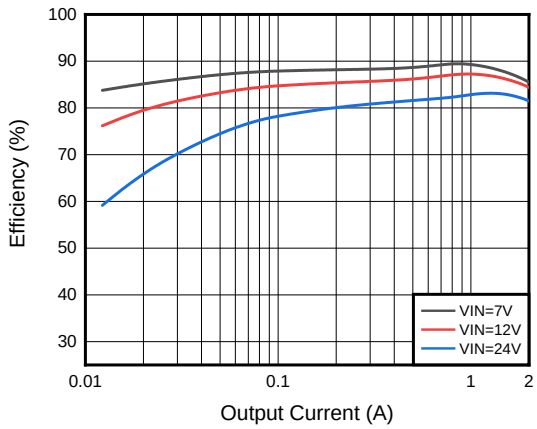


Figure 9. 1.2V Efficiency

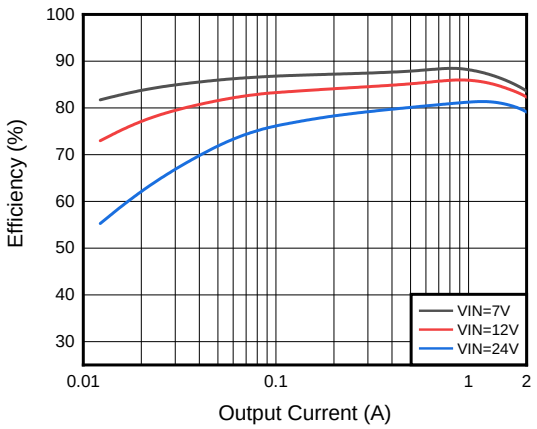


Figure 10. 1.0V Efficiency

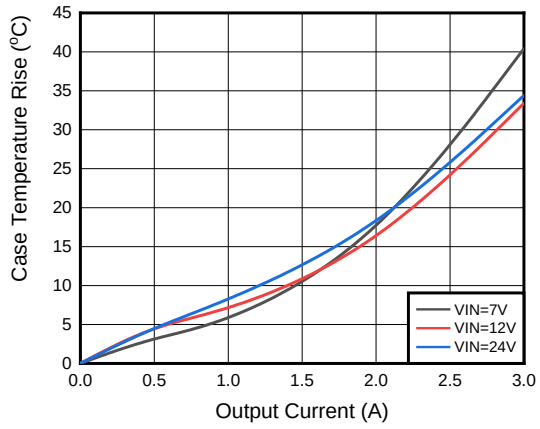


Figure 11. 5V Thermal

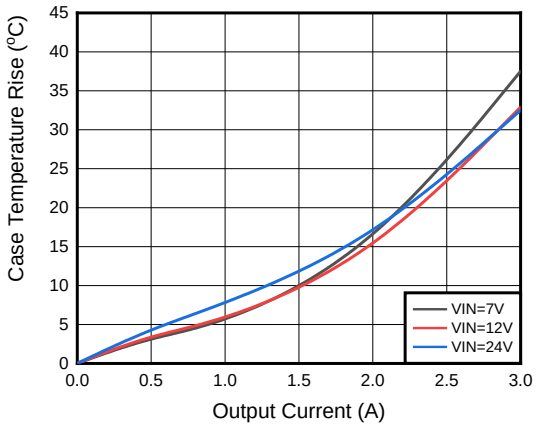


Figure 12. 3.3V Thermal

Typical Characteristic (continued)

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22µF, C_{OUT} = 44µF, L1 = 10µH, and T_A = 25°C, unless otherwise noted.

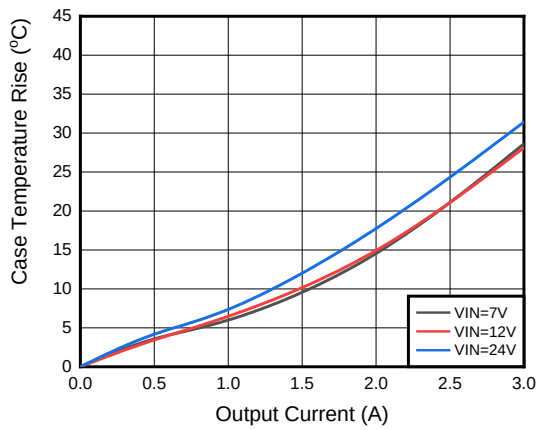


Figure 13. 2.5V Thermal

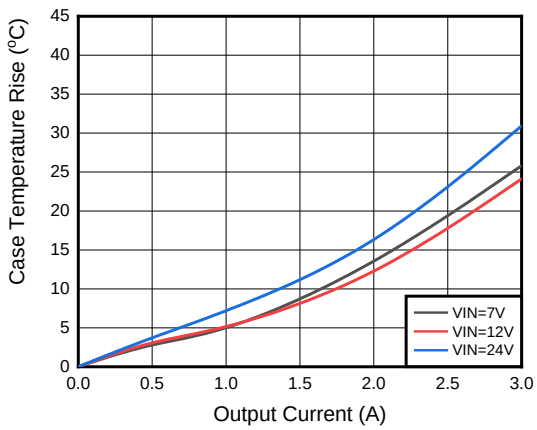


Figure 14. 1.8V Thermal

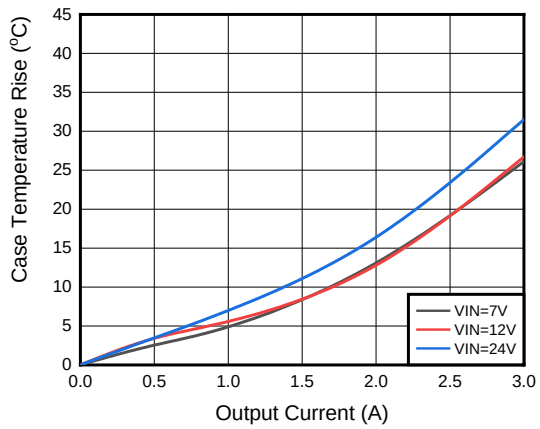


Figure 15. 1.2V Thermal

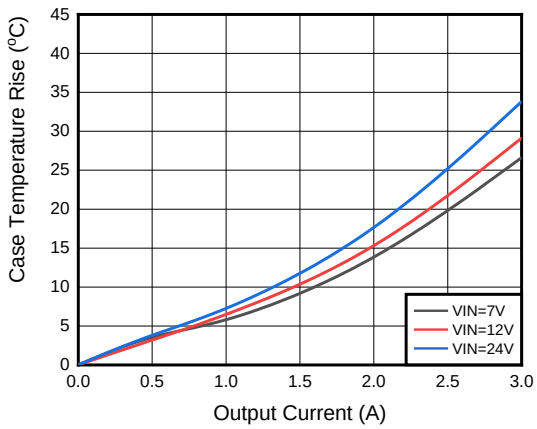


Figure 16. 1.0V Thermal

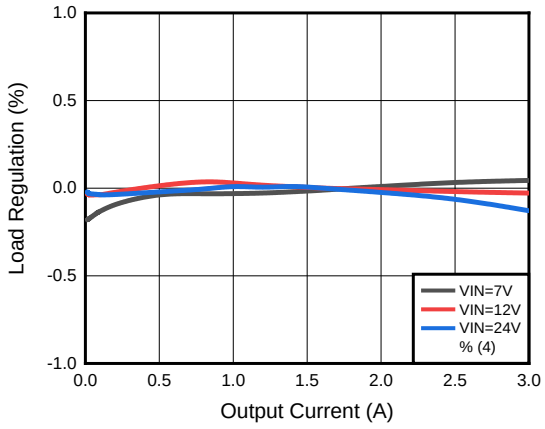


Figure 17. Load Regulation

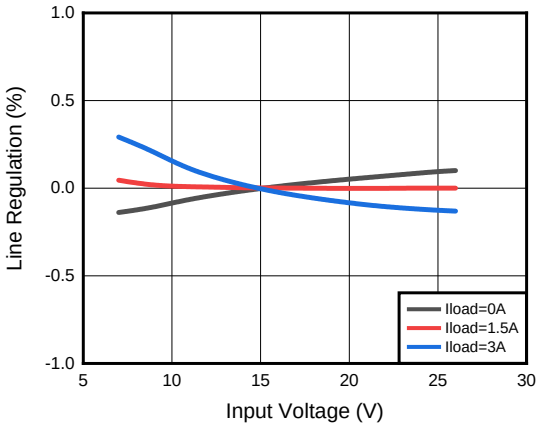


Figure 18. Line Regulation

6 Functional Description

6.1 Block Diagram

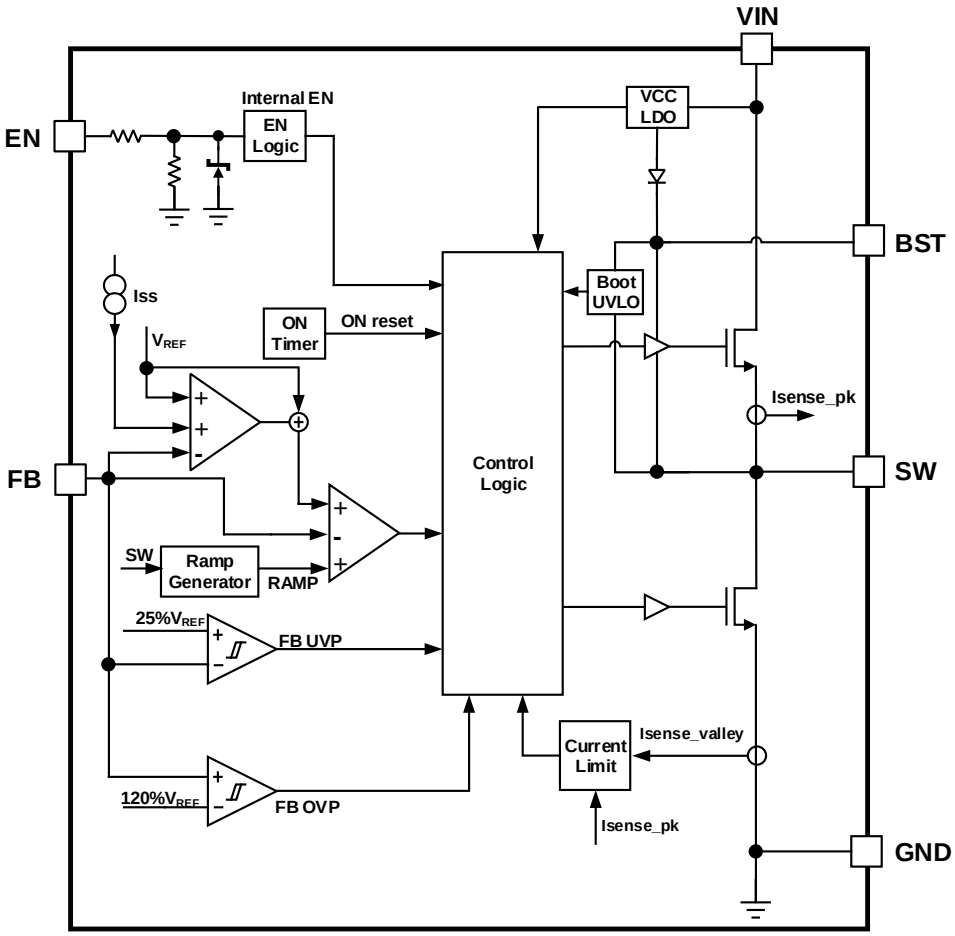


Figure 19. GD30DC135A Functional Block Diagram

6.2 Operation

The GD30DC135A is a synchronous switching step-down converter. The adaptive on-time is so controlled by the input/output voltage that the IC operates at relative constant frequency, typically 600kHz. It is capable of delivering up to 3A for VIN between 4.2V and 28V. The output voltage can be as low as 0.6V.

6.2.1 Pulse-Width Modulation (PWM) Control

The GD30DC135A is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when internal VFB drops

below VREF. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

6.2.2 Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 20). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

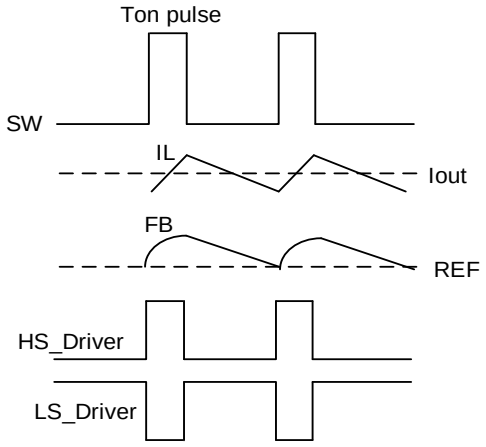


Figure 20. FPFM Operation

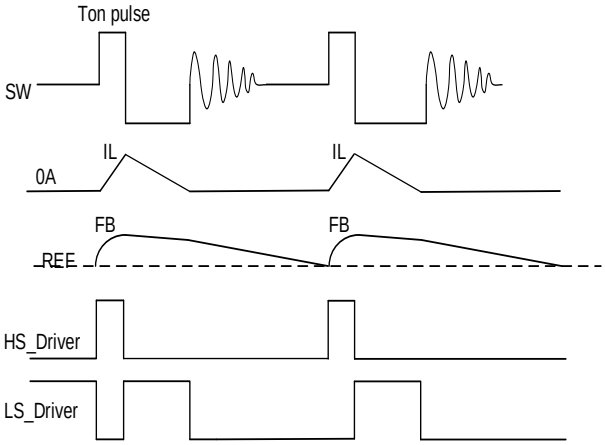


Figure 21. PFM Operation

6.2.3 Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 21. When internal V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, internal V_{FB} cannot reach VREF while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Zi) whenever the inductor current reaches zero. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode

At light-load or no-load condition, the output drops very slowly, and the GD30DC135A reduces the switching frequency naturally. High efficiency is achieved at light load.

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L_{OUT} \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

6.2.4 Soft Startup

After enabling the device, internal soft-start circuitry monotonically ramps up the output voltage which reaches nominal output voltage during a soft-start time of 1.2ms (typical). This avoids excessive inrush current and creates a smooth output voltage rise slope.

6.2.5 Pre-Bias startup

The GD30DC135A is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

6.2.6 Under Voltage Lockout

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The GD30DC135A UVLO comparator monitors the input voltage. The UVLO rising threshold is 4.05V(typical), while its falling threshold is consistently 3.8V.

6.2.7 Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The GD30DC135A has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the LS limit compactor active. The device enters over current protection mode. High side will not be turned on until the valley current limit disappear. Meanwhile, the output voltage drops until V_{FB} is below the under voltage (UV) threshold (typically 30% of the reference). Once UV is triggered, the GD30DC135A enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

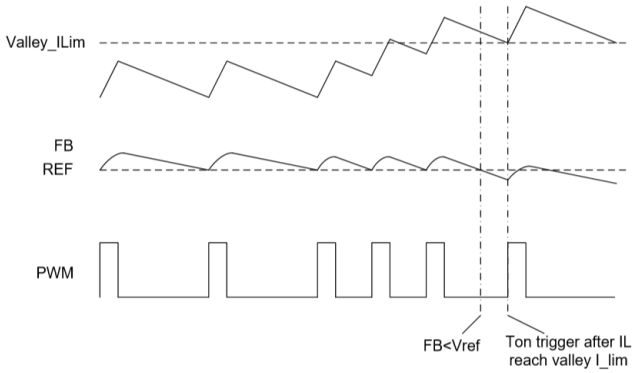


Figure 22. Valley Current Limit Control

6.2.8 Output OVP and UVP

The GD30DC135A monitors a resistor divided V_{FB} to detect over- and under-voltage. When V_{FB} becomes higher than 120%(typical) of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turned off until the negative current (-2.5A typically) limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed. When V_{FB} drops below 25%(typically) of V_{REF}, the UVP comparator output goes high, and the GD30DC135A enters the hiccup protection.

6.2.9 Large Duty Cycle Operation

When GD30DC135A will automatically extend the On time to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The GD30DC135A can support up to 100% maximum duty cycle.

6.2.10 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 25°C (typical), the device returns to normal operation automatically.

6.3 Device Mode Description

6.3.1 Device Enable

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 4.05V), the GD30DC135A can be enabled by pulling EN higher than 1.2V. Leaving EN floating or pulling it down to ground disables the GD30DC135A. There is an internal 0.7MΩ resistor from EN to ground. EN is clamped internally using a 4.5V Zener diode. EN can connected to VIN directly by a resistor.

The EN Pin can connect to VIN by a pull-up resistor, but EN input current need below 100uA. For example, if V_{IN}=24V, the I_{Zener} = (24-4.5) / $R_{PULL-UP}$ < 100uA, So, $R_{PULL-UP}$ > 195KΩ.

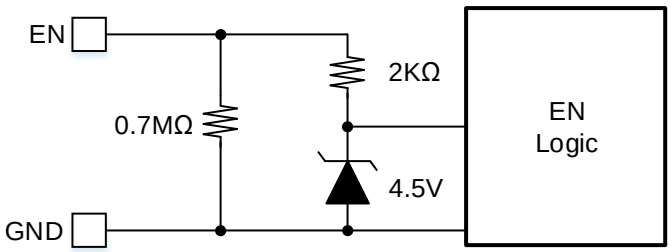


Figure 23. Zener Diode between EN and GND

7 Application Information

7.1 Typical Application Circuit

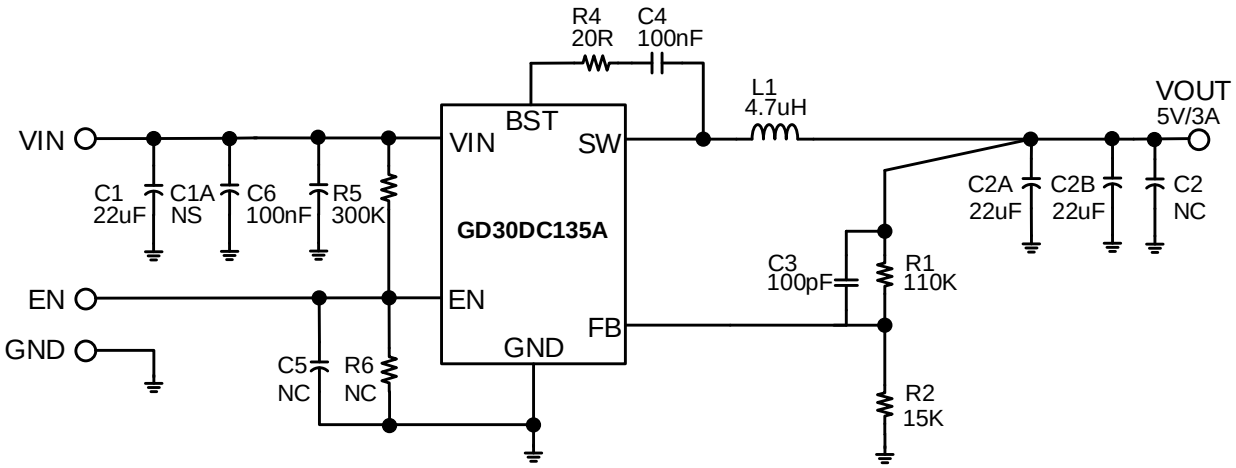


Figure 24. 5.0V, 3A Reference Design

Note: C3 is optional for better transient performance.

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	4.2V to 28V
Output Voltage	5.0V
Maximum Output Current	3A

7.3 Detailed Design Description

7.3.1 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(2). By selecting R1 and R2, the output voltage is programmed to the desired value. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It I recommended to choose a value within 1k to 100k for R2. When the output voltage is regulated, the typical voltage reference at the FB pin is 0.6V.

$$V_{OUT} = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

The feedback circuit is shown in Figure 25.

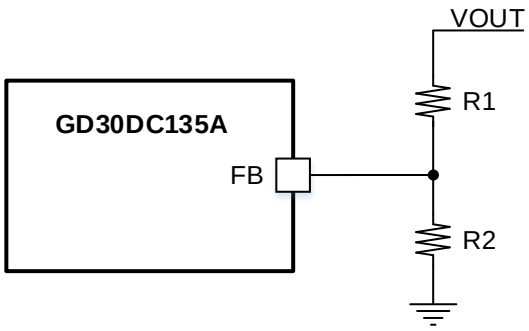


Figure 25. Feedback resistor divider

Table 2 lists the recommended parameters values for common output voltages.

Table 2. Component selection for common output voltages[1,2]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT}(μF)
5	110	15	4.7	44
3.3	67.5	15	4.7	44
2.5	47.5	15	2.2	44
1.8	30	15	2.2	44
1.2	15	15	1.5	44
1	10	15	1.5	44

1. The components used in these design cases do not belong to GD products, GD does not warrant its accuracy or completeness. GD's customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.
2. Refer to *Detailed Design Description* section for guidance on component selection and calculation equations.

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and hight conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(3) and Equation(4). Ensure that the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \tag{3}$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{4}$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(5). Once an inductor value is chosen, the peak inductor current is determined by Equation(4). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (5)$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 22μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(7):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (7)$$

Where D is the duty cycle of converter. The worst-case condition occurs at V_{IN} = 2V_{OUT}. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor, FOSC is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (8)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The GD30DC135A can be optimized for a wide range of capacitance and ESR values.

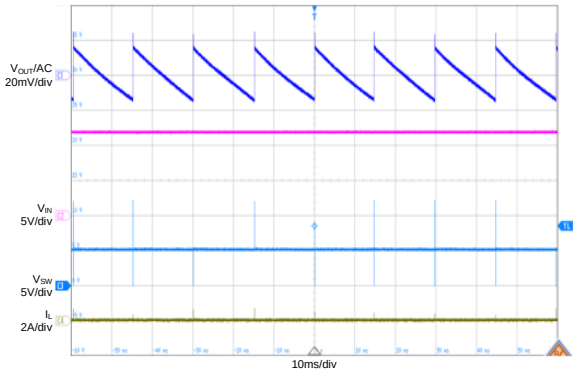
Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value COUT_max can be limited approximately by:

$$C_{OUT\_MAX} = (I_{limitave} - I_{OUT}) \times T_{SS} / V_{OUT} \quad (10)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period, Tss is the soft-start time (1.2ms typically).

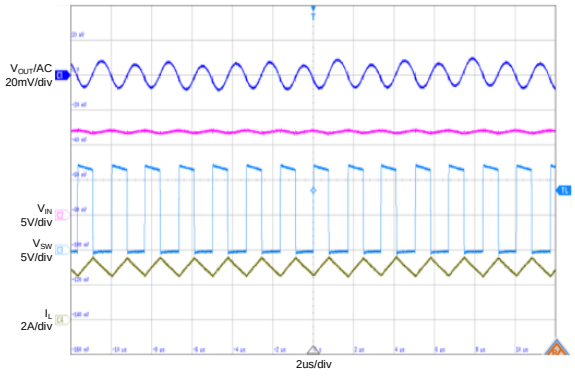
7.4 Typical Application Curves

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 22x2μF, L1 = 4.7μH, and T_A = 25°C, Frequency = 600kHz, unless otherwise noted.



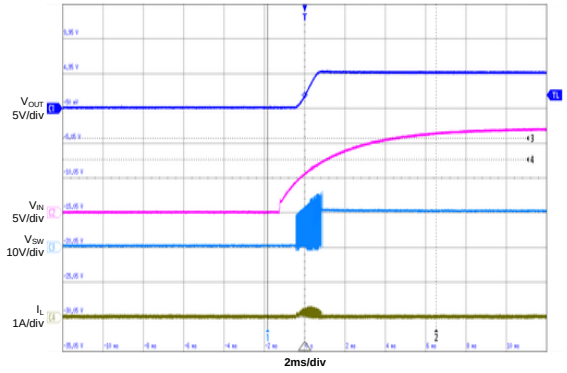
I_{OUT} = 0A

Figure 26.Output Voltage Ripple



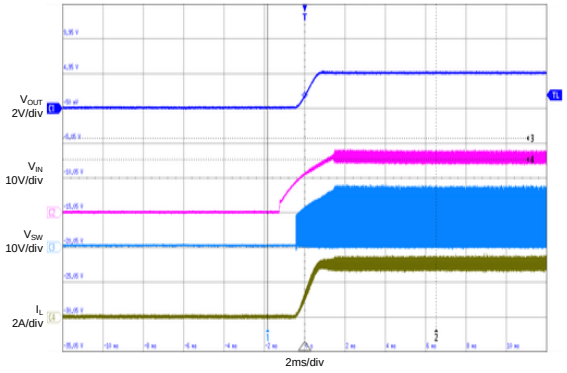
I_{OUT} = 3A

Figure 27.Output Voltage Ripple



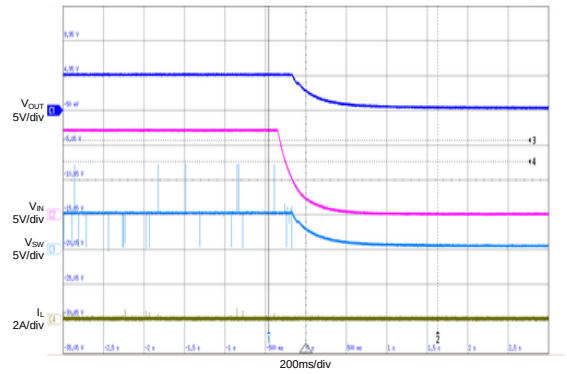
I_{OUT} = 0A

Figure 28.Start-Up through VIN



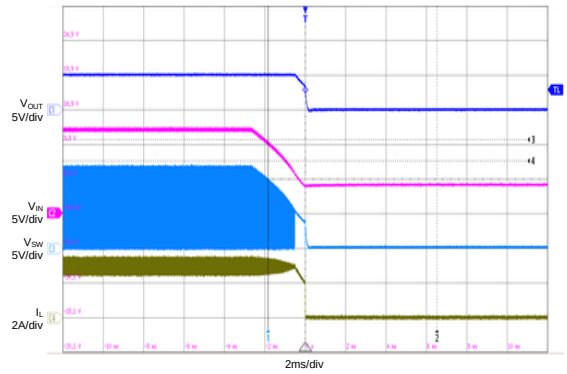
I_{OUT} = 3A

Figure 29.Start-Up through VIN



I_{OUT} = 0A

Figure 30.Shutdown through VIN

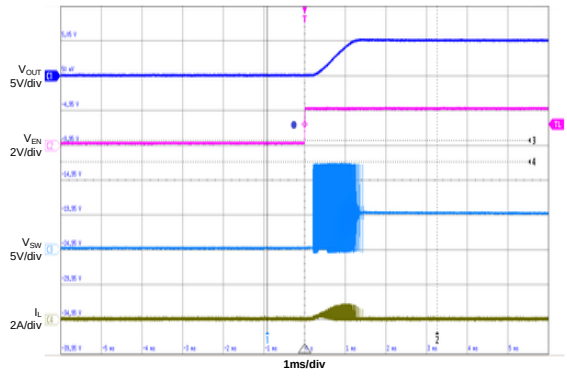


I_{OUT} = 3A

Figure 31.Shutdown through VIN

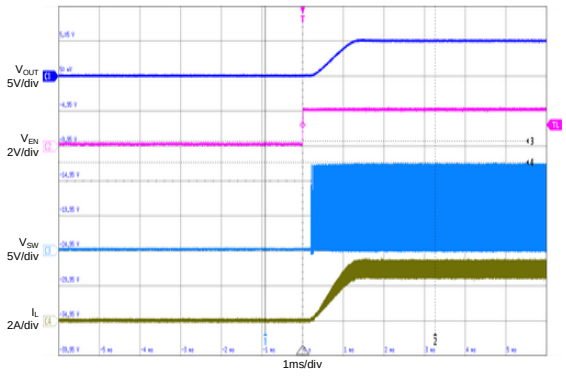
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 22x2μF, L1 = 4.7μH, and T_A = 25°C, Frequency = 600kHz, unless otherwise noted.



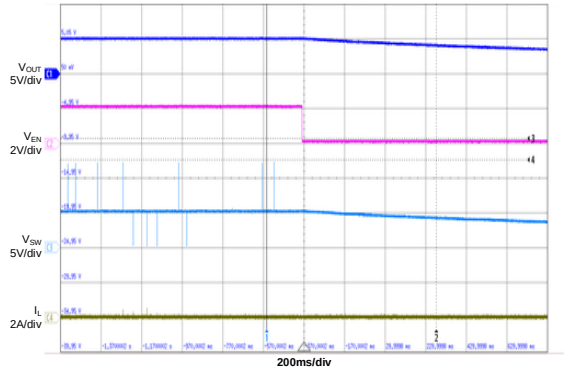
I_{OUT} = 0A

Figure 32.Start-Up through EN



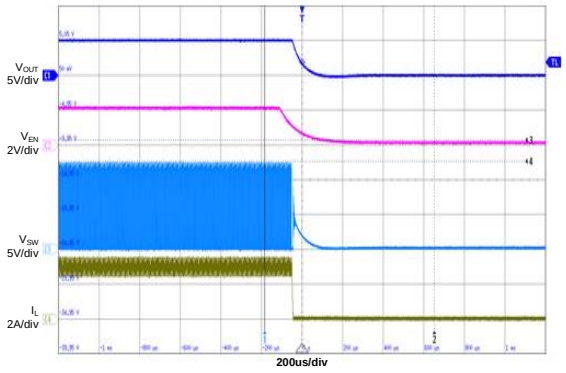
I_{OUT} = 3A

Figure 33.Start-Up through EN



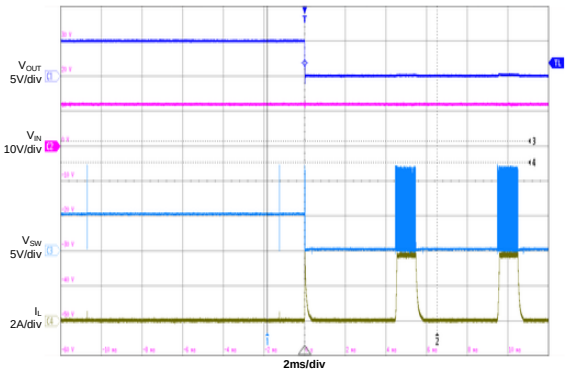
I_{OUT} = 0A

Figure 34.Shutdown through EN



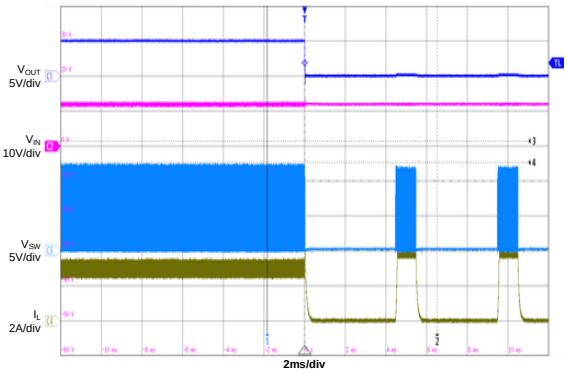
I_{OUT} = 3A

Figure 35.Shutdown through EN



I_{OUT} = 0A

Figure 36.Short Entry

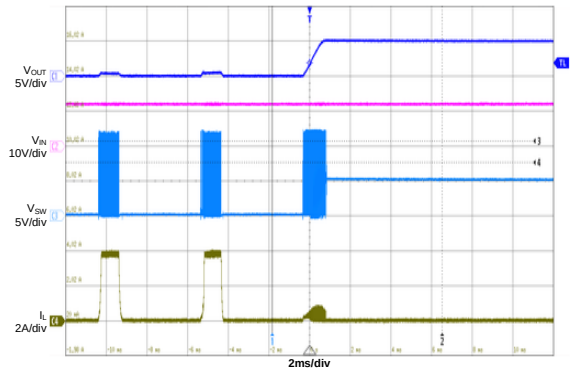


I_{OUT} = 3A

Figure 37.Short Entry

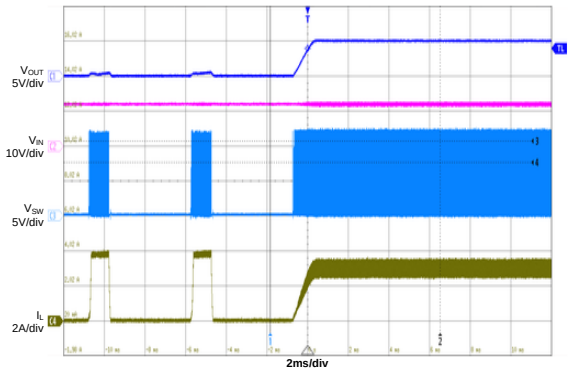
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 22x2μF, L1 = 4.7μH, and T_A = 25°C, Frequency = 600kHz, unless otherwise noted.



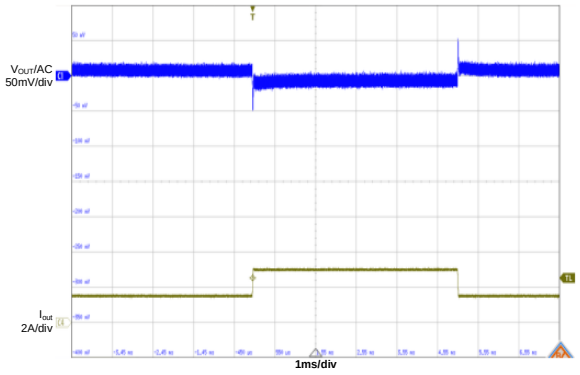
I_{OUT} = 0A

Figure 38.Short Recovery



I_{OUT} = 3A

Figure 39.Short Recovery



I_{OUT} = 1.5A to 3A, 1.2A/us

Figure 40.Load Transient

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

1) Place the input/output capacitor and inductor should be placed as close to IC.
2) Keep the power traces as short as possible.
3) The low side of the input and output capacitor must be connected properly to the power GND avoid a GND potential shift.
4) Place the external feedback resistors next to FB.
5) Keep the switching node SW short and away from the feedback network.

For best results, follow the layout example below.

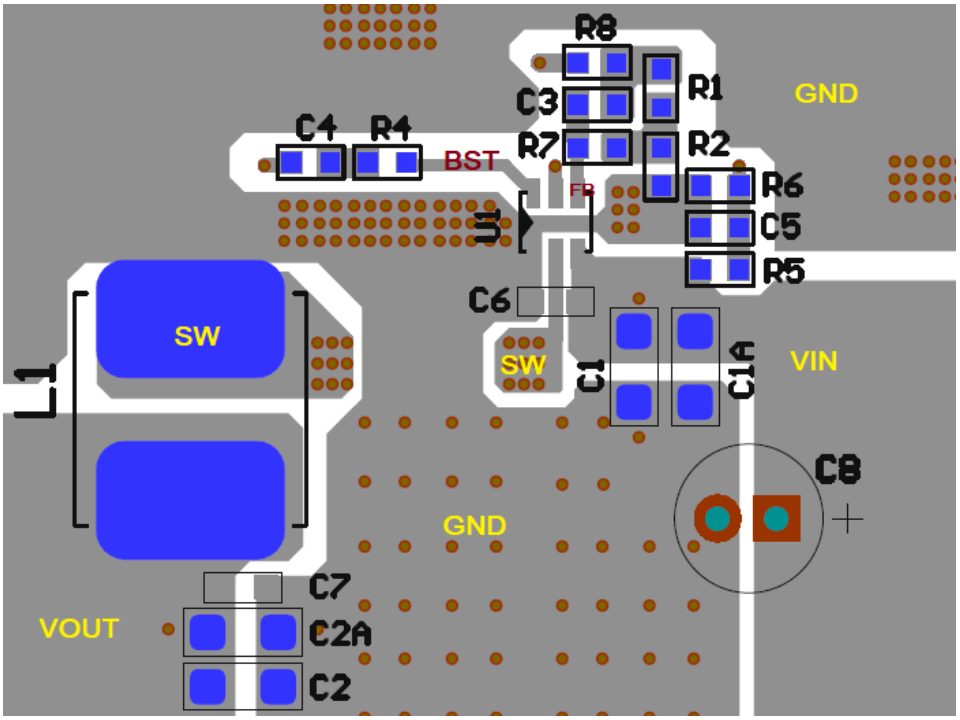


Figure 41. Typical GD30DC135A Example Layout for Top Layer

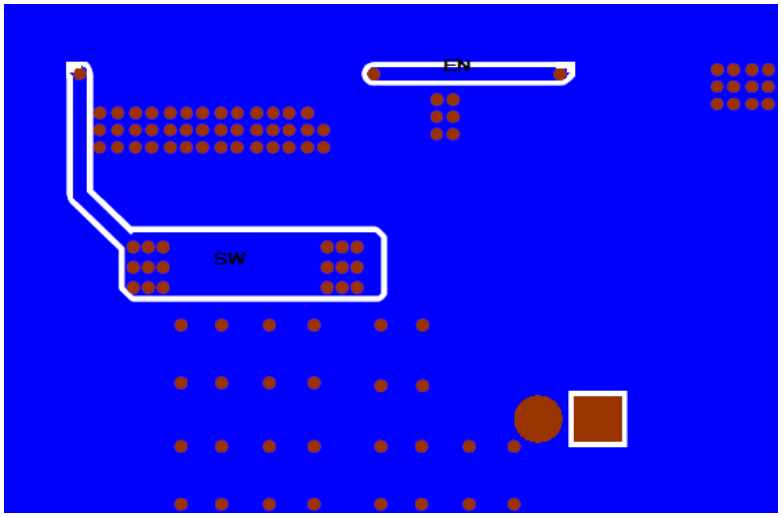
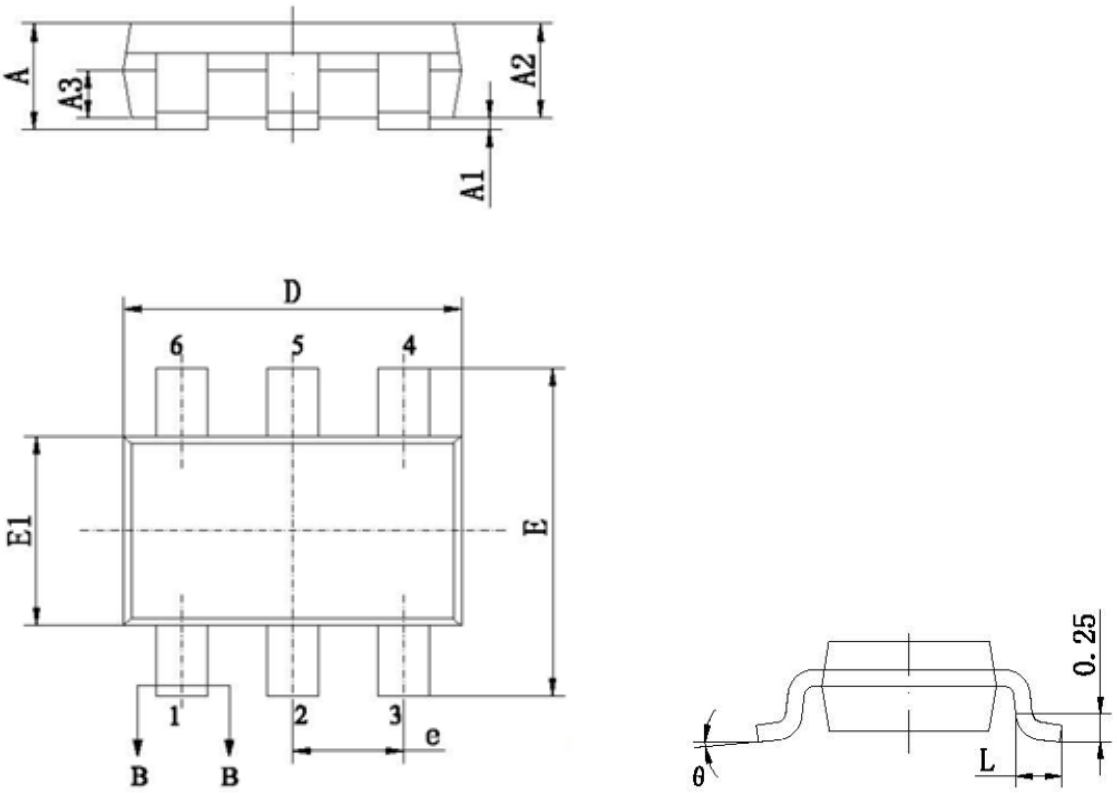


Figure 42. Typical GD30DC135A Example Layout for Bottom Layer

9 Package Information

9.1 Outline Dimensions

SOT23-6 Package Outline



NOTES: (continued)

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *TSOT23-6L dimensions(mm)*.

Table 3. TSOT23-6L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			0.95
A1	0		0.10
A2	0.75	0.80	0.85
A3	0.35	0.40	0.45
b	0.38		0.46
b1	0.37	0.40	0.43
c	0.13		0.17
c1	0.12	0.13	0.14
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
L	0.30	0.40	0.50
θ	0		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC135ASSTR-I	TSOT23-6L	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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