65V, 5A, Step-down Converter with Low-side MOSFET Driver and Programmable Frequency

1 Features

- Wide Input Range: 4.5V to 65V
- Continuous Output Current: 5A
- Integrated High Side NMOS with 80mΩ Low Resistance
- Non-Sync Buck, Sync Buck Selectable by RT/SYNC Pin
- LSG Pin to Drive External LS-FET
- Constant On Time Control
- Low Quiescent Current: 130μA
- 250kHz, 500kHz, 1.2MHz, 2.2MHz Switching Frequency Selectable
- External Frequency Synchronization from 200kHz–1.2MHz
- BIAS Pin to Improve Efficiency
- Low Dropout Mode Support 99.5% Duty Cycle
- Pre-bias Start up
- Available in ESOP8 Package

2 Applications

- 12V, 24V and 48V Power Systems
- Surveillance Camera
- PoE Switch
- Industry applications

3 Description

The GD30DC1602is a 65V, 5A step-down converter which is Integrated high-side power MOSFET with 80mΩ low resistance. Featuring constant on-time (COT) control, the GD30DC1602efficiently delivers up to 5A of output current while ensuring a rapid loop response.

This device optimizes power conversion efficiency across various load conditions by reducing its switching frequency during light loads. This approach minimizes both switching and gate driving losses.

Equipped with essential protection mechanisms, the GD30DC1602 includes a cycle-by-cycle current limit, short-circuit protection with hiccup mode, FB open protection, and thermal shutdown.

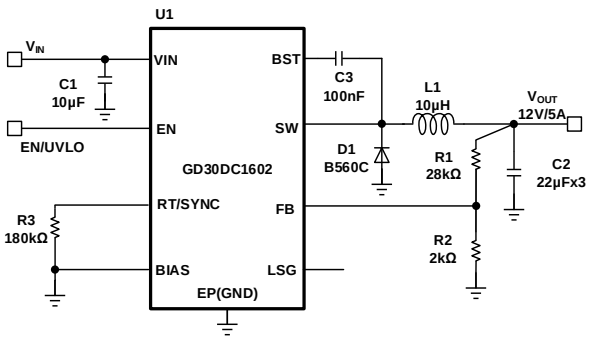
The GD30DC1602 is available with space saving ESOP8 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1602	ESOP8	4.90mm x 3.90mm

1. For packaging details, see *Package Information* section.

Non-Sync buck Application



Sync buck Application

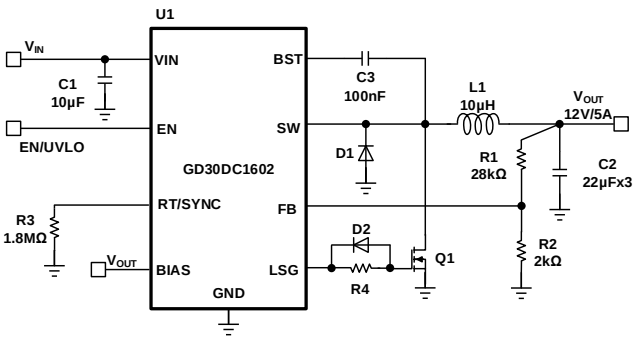
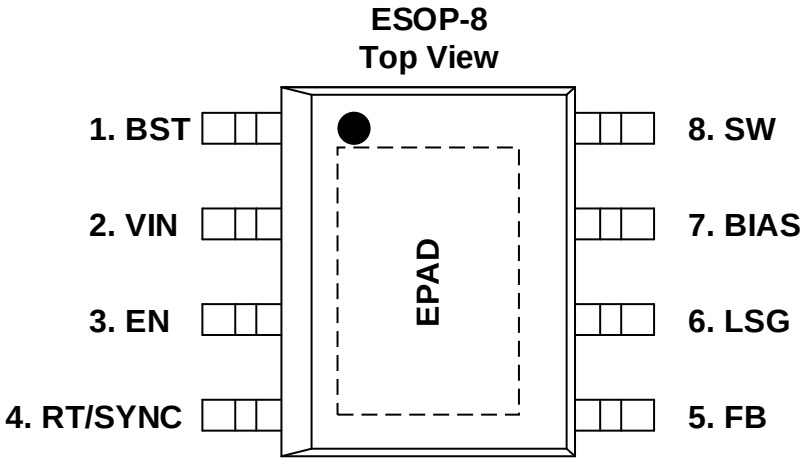


Table of Contents

4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	ESOP8		
BST	1	O	**Bootstrap**. Connect a high-quality BST capacitor between SW and BST to form a floating supply across the high-side switch driver.
VIN	2	P	**Power supply**. Operates from a 4.5V to 70V input rail. Supply input terminal to internal bias LDO and high-side FET. A decoupling capacitor is required to decouple the input.
EN	3	I	**Enable**. Pull high to enable the output. It is internally pulled up via a current source.
RT/SYNC	4	I	**Mode and Frequency Set/External Sync Pin**. Place a resistor between the RT/SYNC and GND pins. Select either an external diode or MOSFET for the low-side. The IC can operate as either a non-synchronous buck or synchronous buck converter, with selectable switching frequencies of 250kHz, 500kHz, 1.2MHz, or 2.2MHz. The switching frequency can be modified by applying an external clock signal to the RT/SYNC pin.
FB	5	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider from VOUT to GND.
LSG	6	I	**External Low Side MOSFET gate driver**. When set up Sync buck, connect LSG pin to external N-MOSFET gate. When set up Non-Sync buck, float this pin.
BIAS	7	P	**External Bias Input of Internal LDO**. Connect the BIAS pin to an external power supply (5V ≤ VBIAS ≤ 20V) through a 4.7Ω resistor to reduce power consumption and improve efficiency. If unused, connect the BIAS pin to GND.
SW	8	O	**Switch output**. Switching node of power stage. Connected to the internal MOSFET switches and inductor terminal.
EPAD	9	G	**Exposed Pad.** Connect the exposed pad to the PCB GND plane to ensure optimal thermal efficiency.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	VIN to GND	−0.3	68	V
V_{EN}	EN to GND	−0.3	68	V
V_{SW}	SW to GND	−0.6	V_{IN}+0.3	V
	SW to GND, Transient 10ns	−9	75	V
V_{BST-SW}	BST to SW	−0.3	6	V
V_{BIAS}	BIAS to GND	−0.3	30	V
V_{LSG}	LSG to GND	−0.3	10	V
All Other Pins		−0.3	6	V
T_{STG}	Storage temperature	−55	150	°C
T_J	Junction temperature	−40	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	VIN to GND	4.5		65	V
V_{OUT}	VOUT to GND	0.8		32	V
V_{BIAS}	BIAS to GND	5		20	V
I_{OUT}	Max Continuous Output Current			5	A
T_J	Junction temperature	−40		125	°C

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	ESOP8	48	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	ESOP8	52	°C/W
$\Theta_{JC(BOT)}$	Junction to case (bottom) thermal resistance	ESOP8	2.3	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN}=48V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO and QUIESCENT CURRENT						
VIN_{UVR}	VIN UVLO rising threshold			4.3		V
VIN_{UVF}	VIN UVLO falling voltage			4		V
VIN_{UVH}	Hysteresis voltage of VIN UVLO			0.3		V
I_Q	Quiescent current	VFB = 0.85V		130		μA
I_S	Shutdown current	VEN = 0V		3		μA
ENABLE						
V_{EN_RISING}	EN rising threshold			1.2		V
$I_{EN\_PULL\_UP}$	EN pulled up current	EN = Low		1.2		μA
		EN = High		5		
I_{EN_HYS}	EN pulled up current hysteresis			3.8		μA
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage		0.791	0.803	0.815	V
V_{FB_UV}	FB UV threshold			0.4		V
T_{OC_DEG}	OC hiccup deglitch time			10		ms
POWER STAGE						
R_{ON_HS}	HS on resistance	V_{BST}-V_{SW} = 5V		80		mΩ
I_{LKG_HS}	HS leakage current	V_{EN} = 0V, V_{SW} = 0V			1	μA
CURRENT LIMIT						
I_{LIMIT_HS}	High side current limit threshold			7.5		A
SOFT START						
T_{SS}	Internal Soft-start time	V_{FB} from 10% to 90%		1.2		ms
SWITCHING FREQUENCY/SYNC FUNCTION						
F_{SW}	Non-Sync buck Switching Frequency	RRT/SYNC = 0kΩ		2200		kHz
		RRT/SYNC = 91kΩ		1200		kHz
		RRT/SYNC = 180kΩ		500		kHz
		RRT/SYNC = 430kΩ		250		kHz

Electrical Characteristics (continued)

V_{IN}=48V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW}	Sync buck Switching Frequency (FPWM mode)	RRT/SYNC = 820kΩ		1200		kHz
		RRT/SYNC = 1.8MΩ		500		kHz
		RT/SYNC pin float		250		kHz
F_{SYNC}	External clock		0.2		1.2	MHz
T_{SYNC_MIN}[1]	Min Sync Pulse Width			20		ns
V_{IH_SYNC}	SYNC Input Voltage Threshold			1.55	2	V
V_{IL_SYNC}			0.5	1.2		V
T_{ON_MIN}[1]	Min On pulse			120		ns
T_{ON_MAX}[1]	Max On pulse			40		μs
T_{OFF_MIN}[1]	Min Off time	Non-Sync buck		140		ns
LSG						
V_{LSG}	LSG High Level voltage			6.7		V
I_{SOURCE}	LSG Source current			120		mA
R_{LOW}	LSG Pull-down resistor			1.4		Ω
THERMAL PROTECTION						
T_{OTP_R}[1]	Thermal Shutdown Entry			160		°C
T_{OTP_F}[1]	Thermal Shutdown Recovery			140		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

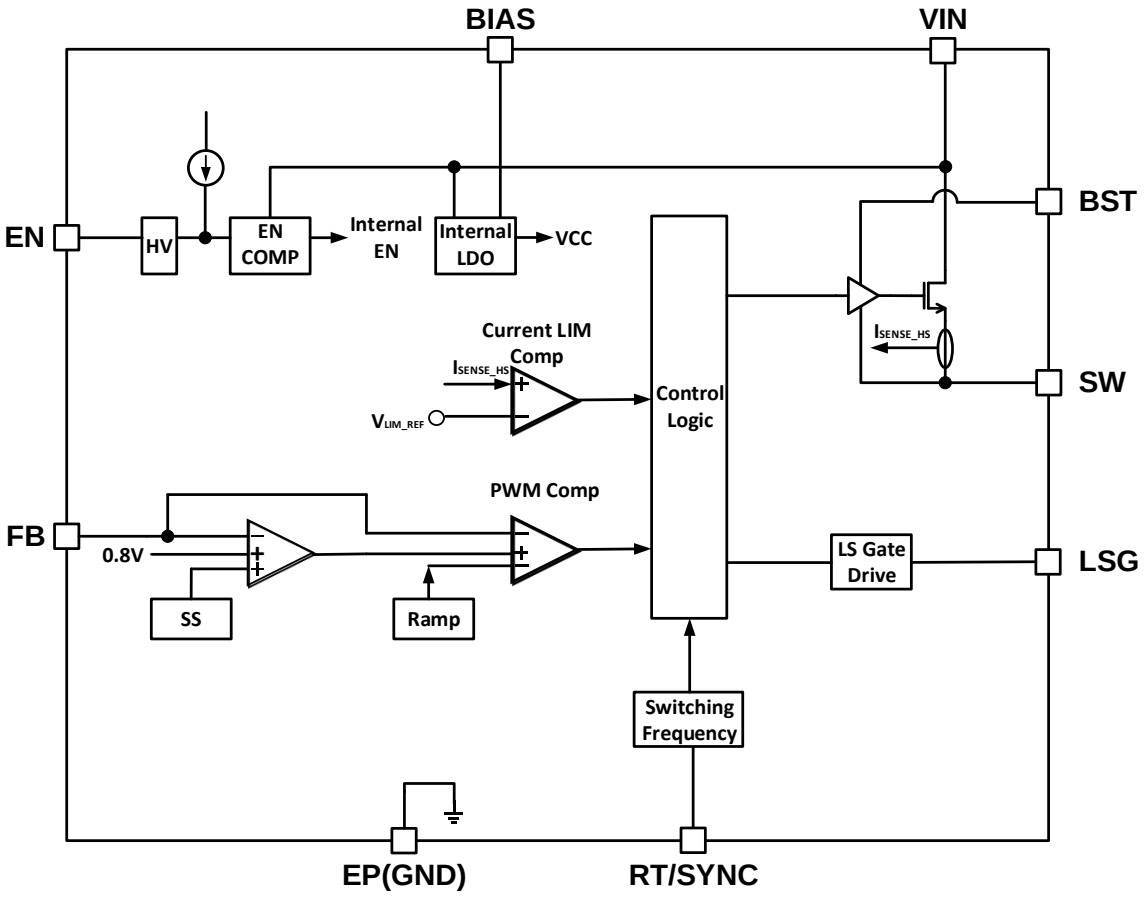


Figure 1. GD30DC1602 Functional Block Diagram

6.2 Pulse-Width Modulation (PWM) Operation

The GD30DC1602 is a fully integrated non-synchronous step-down converter. It utilizes constant-on-time (COT) control to achieve fast transient response and simplify loop stabilization. At the start of each cycle, the high-side MOSFET (HS-FET) is activated when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), signaling that the output voltage is insufficient. The on-time duration is determined by both the input and output voltages, ensuring relatively stable switching frequency across the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. Through this repetitive process, the converter regulates the output voltage.

To enhance stability, internal compensation is integrated with the COT control, enabling stable performance even when ceramic capacitors are used for output. This internal mechanism also improves jitter performance without affecting the line or load regulation.

6.2.1 Non-Sync Buck Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current remains above zero amps (see Figure 2). When the V_{FB} falls below the V_{REF}, the HS-FET turns on for a fixed duration controlled by the one-shot timer. Once the HS-FET switches off, the external free-wheeling diode carries the current.

In CCM, the switching frequency remains relatively stable, a behavior known as pulse-width modulation (PWM) mode.

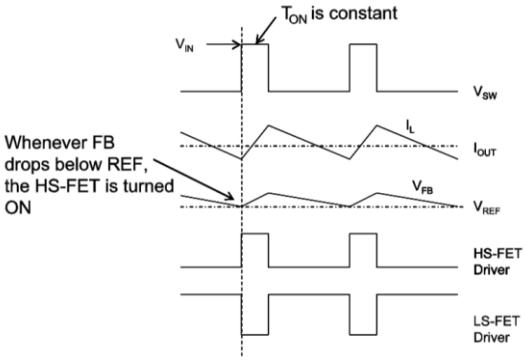


Figure 2. Heavy-Load Operation

6.2.2 Non-Sync Buck Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM). Light-load operation is shown in Figure 2. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the free-wheeling diode is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The free-wheeling diode will shut down the negative current and IC goes into tri-state. The output capacitor discharge to GND through the feedback resistor slowly. So the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode. High efficiency is achieved in light-load condition.

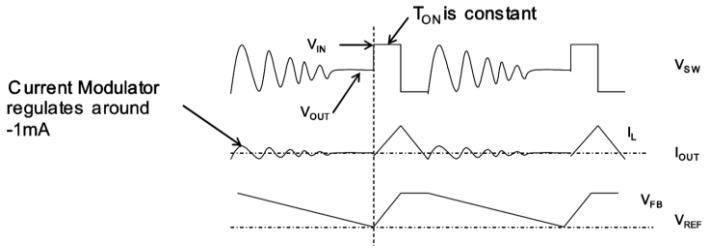


Figure 3. Light-Load Operation

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation shown below:

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

6.2.3 Sync Buck Application

GD30DC1602 has a LSG pin which can be used to drive the external N-MOSFET as the Buck converter LS-FET. If use LSG pin, need to set the resistor between RT/SYNC and GND larger than 800kΩ or float RT/SYNC pin. The whole circuit will work as Sync buck. IC will work in FPWM mode.

In FPWM mode, IC switching frequency is fairly consistent with load current changing, this will help to minimize light-load V_{OUT} ripple, meantime ease the second stage filter design to damp the power stage noise, another side, due to internal power HS-FET on and off more frequently, the light-load efficiency is lower than PFM mode.

When work as Sync buck, an internal 120mA current will charge the external LS-FET gate to high-level voltage 6V (typical). An external LS-FET which's Qg is less than 30nC with 1.4V to 2.5V Vth is recommended to achieve better efficiency. Also recommend to connect BIAS pin to V_{OUT} through a 4.7Ω resistor when V_{OUT} is between 5V and 20V to achieve better efficiency. Need to parallel a schottky diode between SW and GND for stability. A SOD-123 package of DSS210 schottky diode is recommended.

If need a resistor which is larger than 0Ω to limit external mosfet's gate speed, a parallel schottky diode is necessary. Refer to section "Typical Application Circuits".

6.2.4 Internal LDO and BIAS

Most of the internal circuitry is powered by a 5V output internal LDO. This LDO bears voltage from V_{IN} to 5V. When V_{IN} exceeds 5V, the LDO maintain 5V output. When V_{IN} falls below 5V, the output decreases following V_{IN}. For better efficiency and thermal performance, connect BIAS to V_{OUT} through a 4.7Ω resistor, V_{OUT} should between 5V and 20V. In this case the BIAS pin will supply the LSG to drive external LS-FET to improve the efficiency and reduce LDO dissipation. Connect BIAS pin to GND if not use.

6.2.5 Switching Frequency and External Clock Synchronization

The RT/SYNC PIN can determine the switching frequency and working mode. When set up Non-Sync buck, need to connect the schottky diode between SW and GND. When LSG pin is used, need to connect the external N-MOSFET as the Buck converter LS-FET.

Table 1. Design Parameters Switching frequency set resistor selection

RT/SYNC PIN	Topology/Mode	Switching Frequency
RT/SYNC short to GND	Non-Sync buck	2200kHz
RT/SYNC=91kΩ		1200kHz
RT/SYNC=180kΩ		500kHz
RT/SYNC=430kΩ		250kHz
RT/SYNC=820kΩ	Sync buck FPWM mode	1200kHz
RT/SYNC=1.8MΩ		500kHz
RT/SYNC float		250kHz

The RT/SYNC terminal can receive a frequency synchronization signal from an external system clock. The square wave applied to the RT/SYNC terminal must switch lower than 0.5V and higher than 2V and have a pulse width

greater than 20ns. The synchronization frequency range is 200 kHz to 1200kHz. During the transition from the external synchronization mode to the resistor programmed mode, the switching frequency will fall to 250kHz and then increase or decrease to the resistor programmed frequency when the 0.5V bias voltage is reapplied to the RT/SYNC resistor.

6.2.6 Under-Voltage Lockout (UVLO) and Enable (EN) Control

The GD30DC1602 is enabled when the VIN terminal voltage rises above 4.3V and the EN terminal voltage exceeds the enable threshold of 1.2V. The GD30DC1602 is disabled when the VIN terminal voltage falls below 4V or when the EN terminal voltage is below 1.2V. The EN terminal has an internal pull-up current source, IEN_PULL_UP, of 1.2μA that enables operation of the GD30DC1602 when the EN terminal floats.

For the application which requires a higher under voltage lockout (UVLO) threshold, use the circuit shown below to adjust the input voltage UVLO with two external resistors. When the EN terminal voltage exceeds 1.2V, an additional 3.8μA of hysteresis current, IEN¬_HYS, is sourced out of the EN terminal. When the EN terminal is pulled below 1.2V, the 3.8μA IEN_HYS current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use below equation to calculate RUVLO1 for the desired UVLO hysteresis voltage and RUVLO2 for the desired VIN start voltage Enable (EN) is a digital control pin that turns the regulator on and off. Refer below for the calculation equation:

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{EN_{HYS}}} \quad (2)$$

$$R_{UVLO2} = \frac{1.2V}{\frac{V_{START} - 1.2V}{R_{UVLO1}} + I_{EN_{PULL\_UP}}} \quad (3)$$

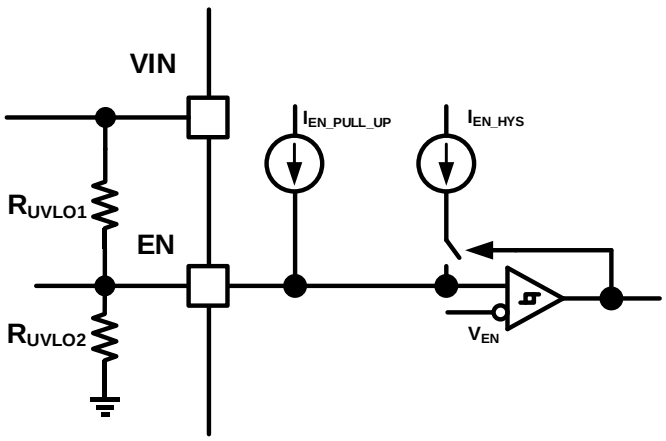


Figure 4. Adjust the Under Voltage Lockout

6.2.7 Internal Soft Start (SS)

The soft-start (SS) function prevents output voltage overshoot during start-up. When the chip powers on, the internal circuit generates a soft-start voltage (V_{SS}) that gradually increases from 0V to 1V. While V_{SS} remains below V_{REF}, V_{SS} replaces V_{REF} as the reference for the error amplifier. Once V_{SS} surpasses V_{REF}, the error amplifier switches back to using V_{REF}. The soft-start duration is internally set to 1.2ms.

6.2.8 High Duty Mode Operation

GD30DC1602 will automatically extend the on time to support the application when VIN is close to VOUT. The on time extend circuit will be triggered when $T_{OFF-MIN}$ time is reached. The GD30DC1602 can support up to 99.5% maximum duty cycle.

6.2.9 Current limit and Short protection

The GD30DC1602 has a peak current limit. During HS-FET on, the inductor current is monitored. If the sensed inductor current reaches the peak current limit after blanking time, the HS-FET would be turn off. The maximum current of the HS-FET is limited cycle-by-cycle internally. Besides, when the output is short, GD30DC1602 will auto fold back the switching frequency to prevent the current from runaway, to make system reliable.

6.2.10 Pre-Bias Start-Up

The GD30DC1602 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

6.2.11 Thermal Shutdown

The thermal shutdown feature protects the chip from excessive temperatures. If the silicon die temperature exceeds 160°C, the chip automatically powers down. It reactivates once the temperature drops below the lower threshold, typically 140°C.

7 Application Information

7.1 Typical Application Circuit

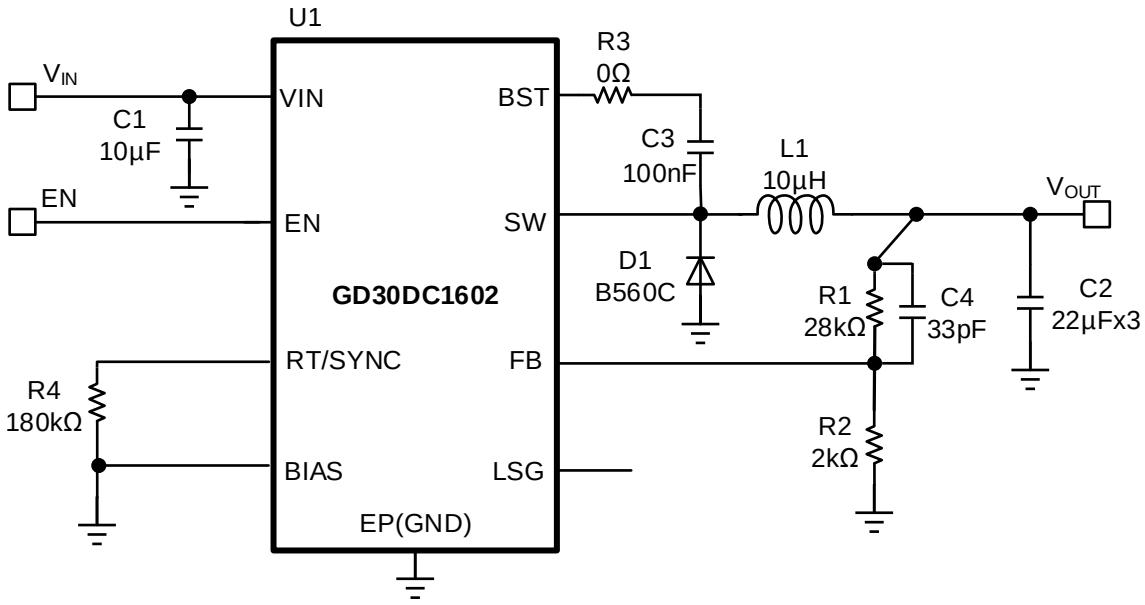


Figure 5. V_{IN}=48V, V_{OUT}=12V/5A, Non-Sync buck, F_{SW}=500kHz[1]

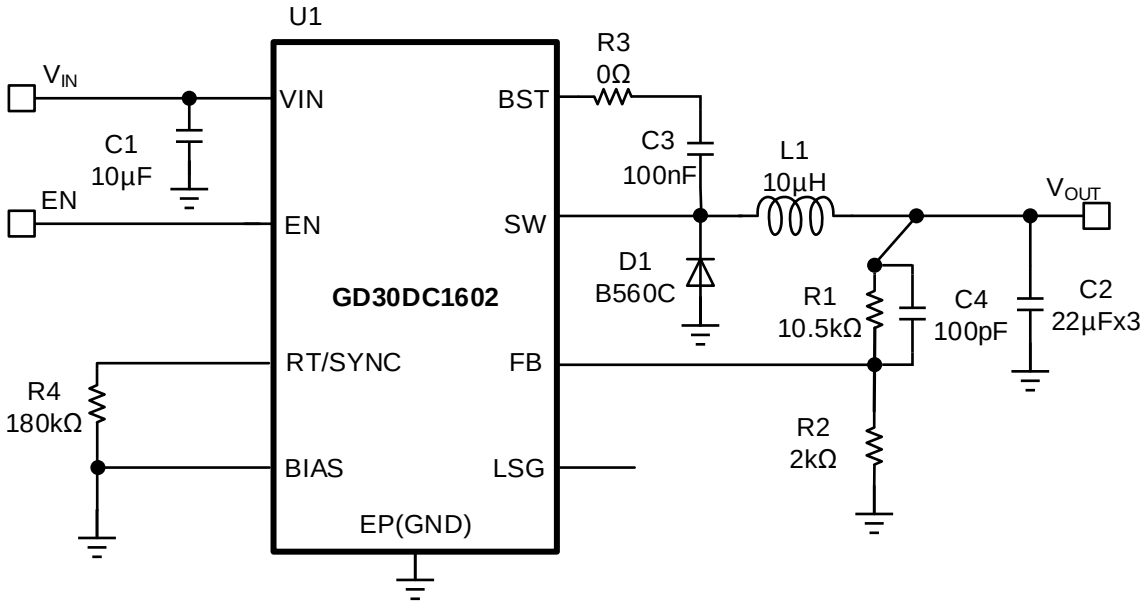


Figure 6. V_{IN}=48V, V_{OUT}=5V/5A, Non-Sync buck, F_{SW}=500kHz[1]

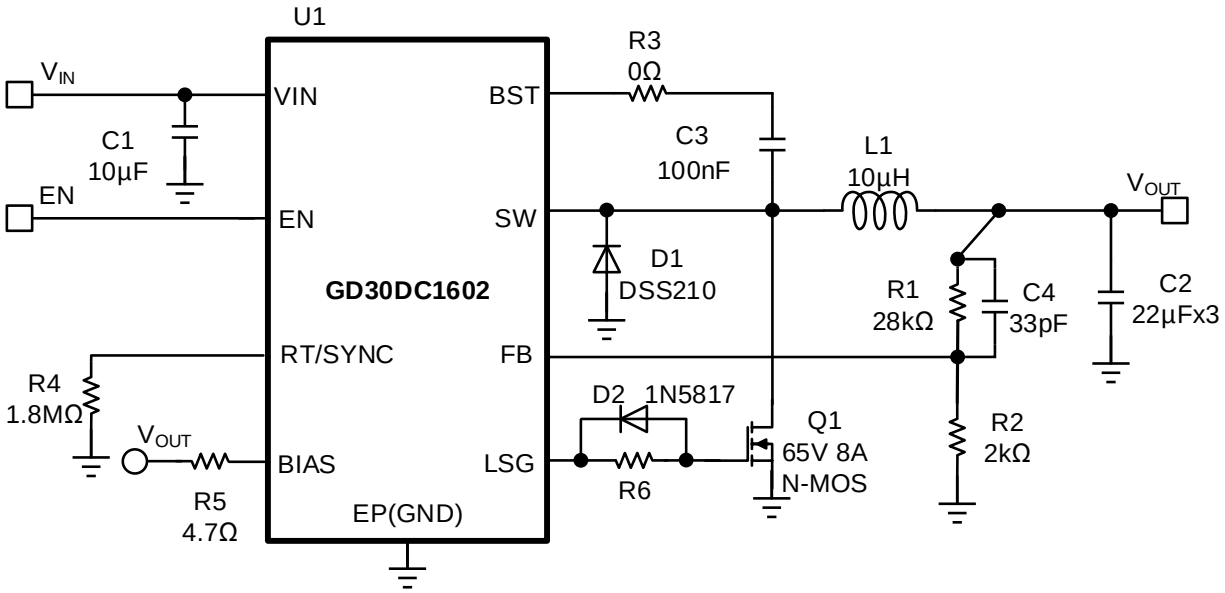


Figure 7. V_{IN}=48V, V_{OUT}=12V/5A, Sync buck, F_{SW}=500kHz[1, 2]

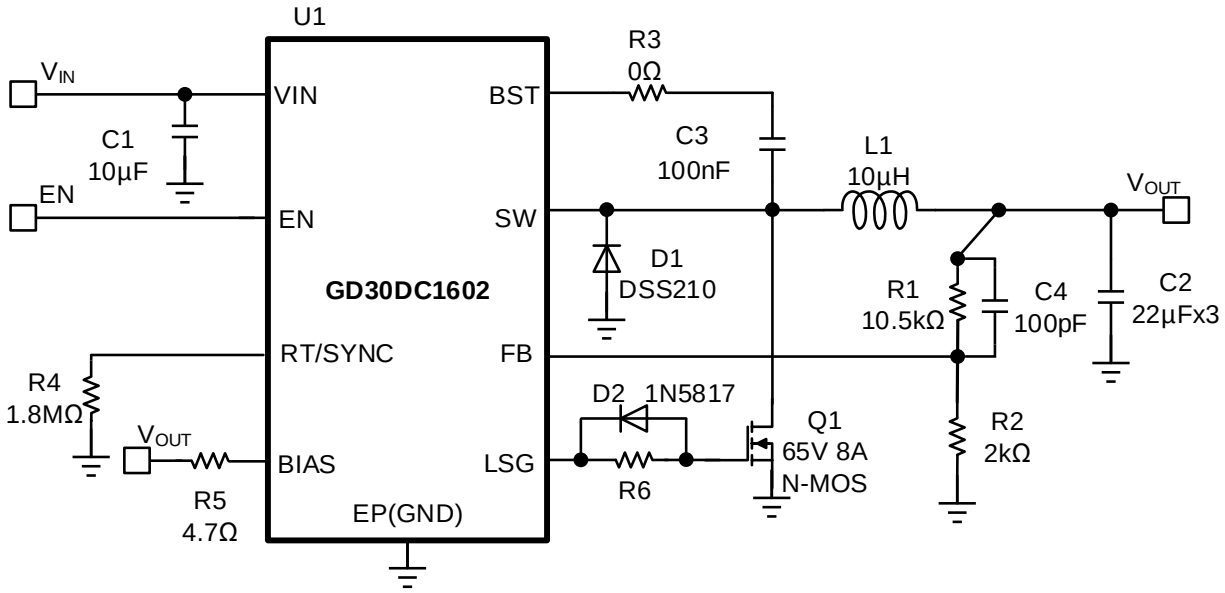


Figure 8. V_{IN}=48V, V_{OUT}=5V/5A, Sync buck, F_{SW}=500kHz[1,2]

1. C4 is optional for better transient performance
2. A parallel schottky diode(D2) is necessary when R6>0Ω.

7.2 Detailed Design Description

7.2.1 Setting the Output Voltage

The GD30DC1602 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.803V. The feedback network is shown below Figure.

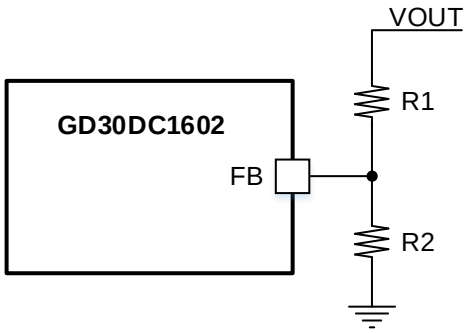


Figure 9. Feedback resistor divider

Choose R1 and R2 using Equation(4):

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \quad (4)$$

7.2.2 Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from Equation(5):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (5)$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation(6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2. Resistor Selection for Common Output Voltages[1]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff} (pF)	L (μH)	C_{OUT} (μF)
12	28	2	33(optional)	10	66
5	10.5	2	100(optional)	10	66

1. For a detailed design circuit, please refer to the Typical Application Circuits

7.2.3 Selecting the Output Capacitor

The output capacitor (C2, C3) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation(7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The GD30DC1602 can be optimized for a wide range of capacitance and ESR values.

7.2.4 Selecting LS-FET

If use GD30DC1602 as Sync buck, a N-MOSFET which Q_g is less than 20nC with 1.4V to 2.5V $V_{GS(th)}$ is recommended to achieve better efficiency. There are some MOSFET recommendation.

Table 3. LS-FET Recommendation[1]

Manufacturer	Part Number	V_{DS}	ID	$R_{DS(ON)}$	Q_g	$V_{GS(th)}$
WINSEMI	SEG9599AG	100V	23A	19.5mΩ (VGS=10V)	22.7nC (VGS=10V)	1.8V
MCC	MCAC38N10YHE3	100V	38A	15mΩ (VGS=10V)	16nC (VGS=10V)	1.8V
APM	APG40N10S	100V	40A	19mΩ (VGS=10V)	16.2nC (VGS=10V)	1.5V

1. All the parameter is typical value.

7.3 Typical Application Curves

V_{IN} = 48V, V_{OUT} = 12V, Non-Sync buck, f_{SW} = 500kHz, C_{IN} = 4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

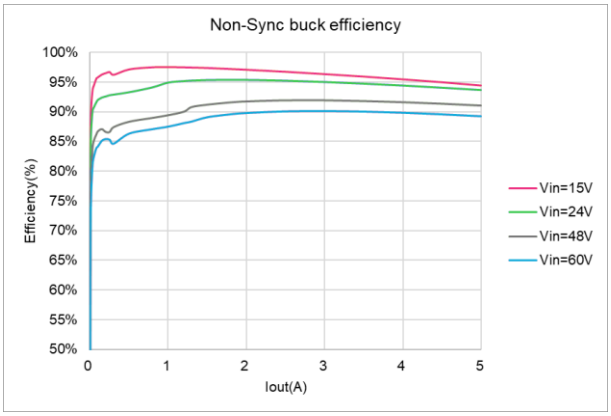


Figure 10. Efficiency vs. Load Current (V_{OUT}=12V, L=10μH, DCR=10mΩ)

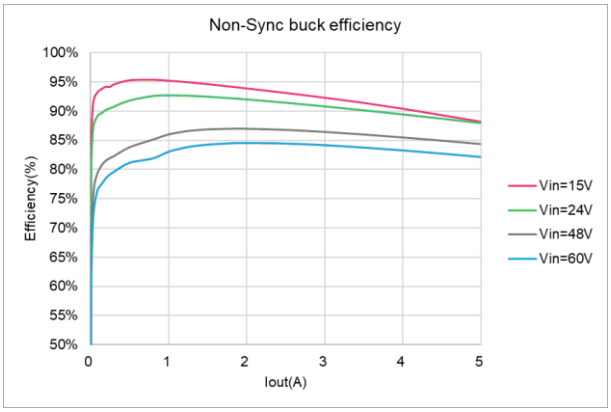


Figure 11. Efficiency vs. Load Current (V_{OUT}=5V, L=10μH, DCR=10mΩ)

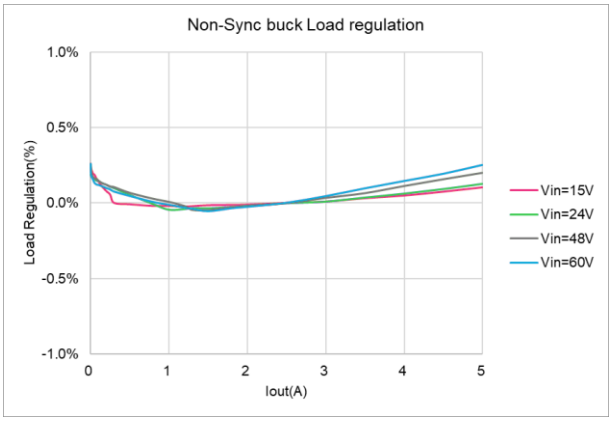


Figure 12. Load Regulation

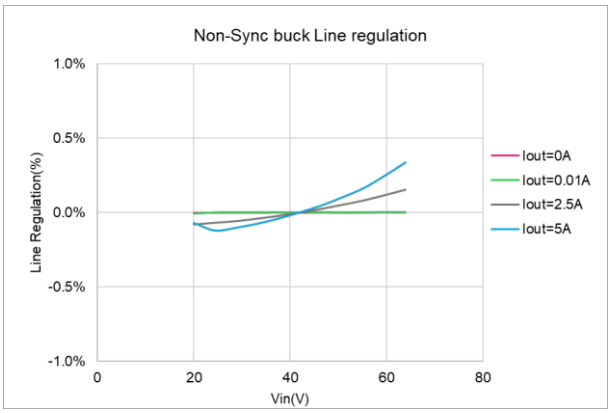


Figure 13. Line Regulation

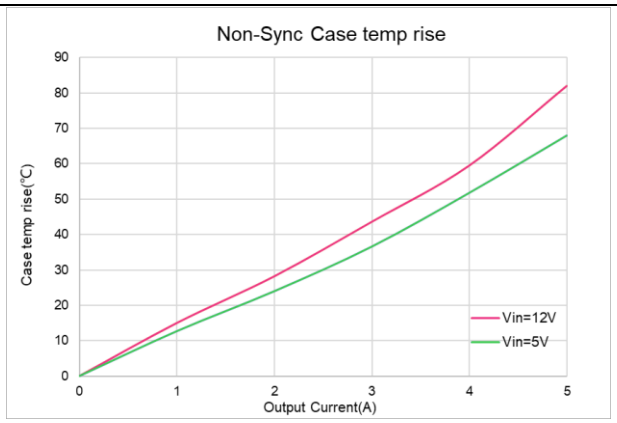


Figure 14. Thermal (No air flow)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Sync buck, f_{SW} = 500kHz, C_{IN} = 4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

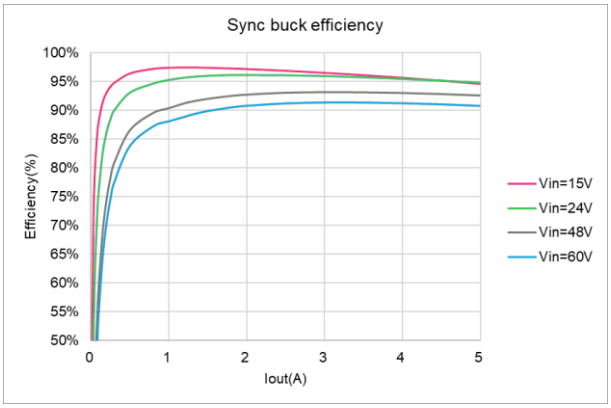


Figure 15. Efficiency vs. Load Current (V_{OUT}=12V, L=10μH, DCR=10mΩ)

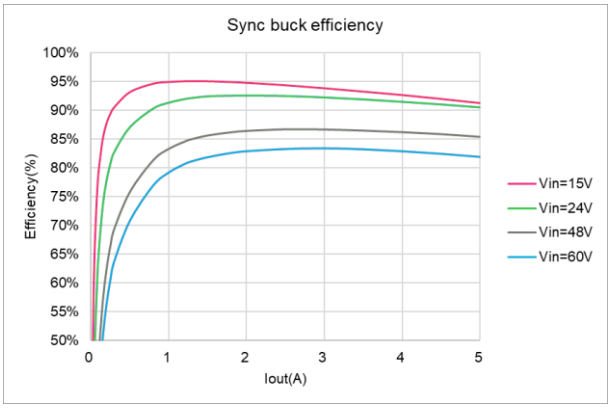


Figure 16. Efficiency vs. Load Current (V_{OUT}=5V, L=10μH, DCR=10mΩ)

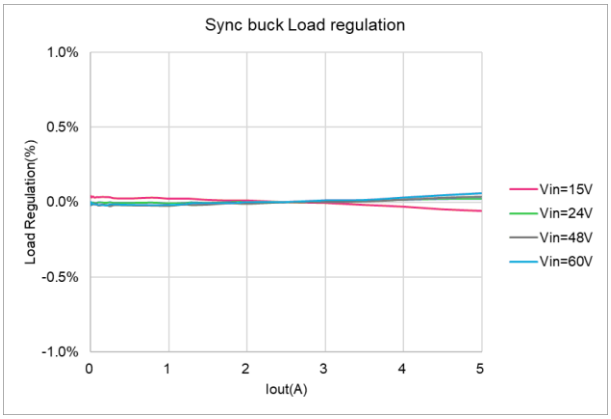


Figure 17. Load Regulation (V_{OUT}=12V)

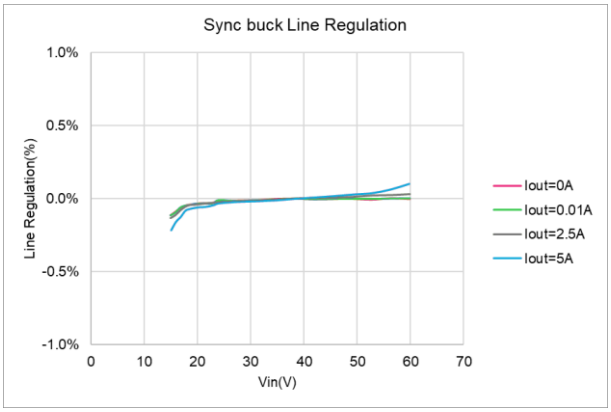


Figure 18. Line Regulation (V_{OUT}=12V)

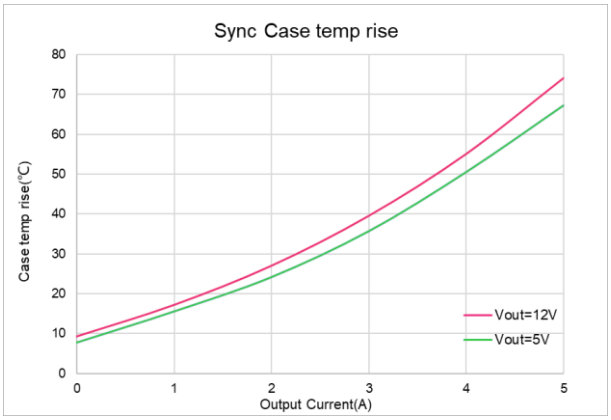


Figure 19. Thermal (No air flow)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Non-Sync buck, f_{SW} = 500kHz, C_{IN} = 4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

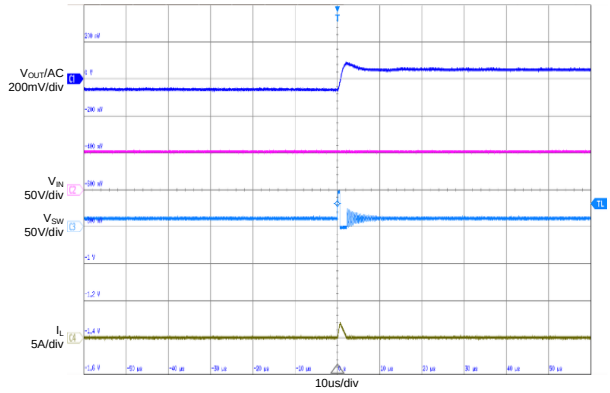


Figure 20. Output Voltage Ripple (I_{OUT} = 0A)

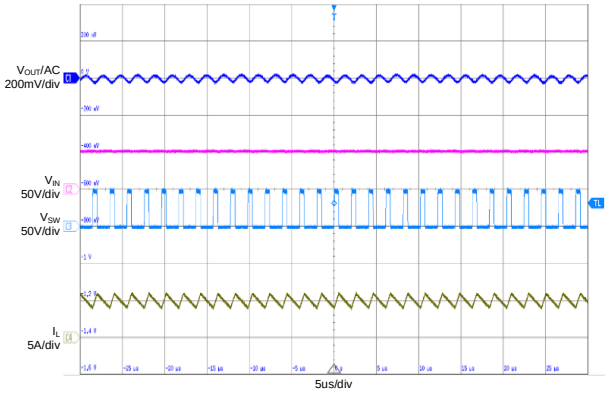


Figure 21. Output Voltage Ripple (I_{OUT} = 5A)

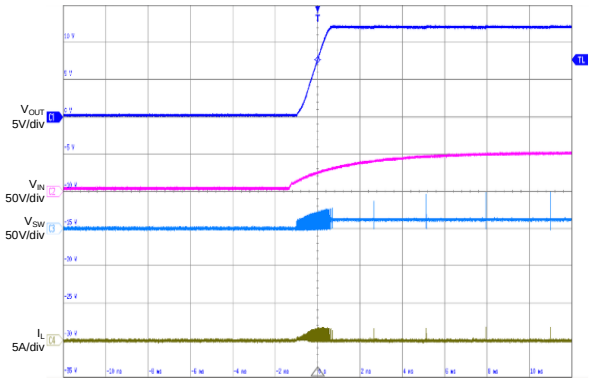


Figure 22. Startup through V_{IN} (I_{OUT} = 0A)

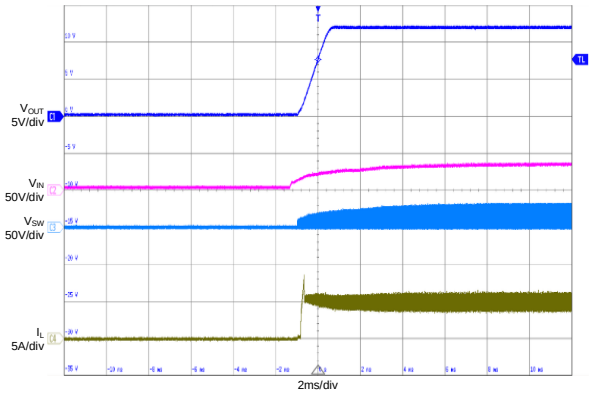


Figure 23. Startup through V_{IN} (I_{OUT} = 5A)

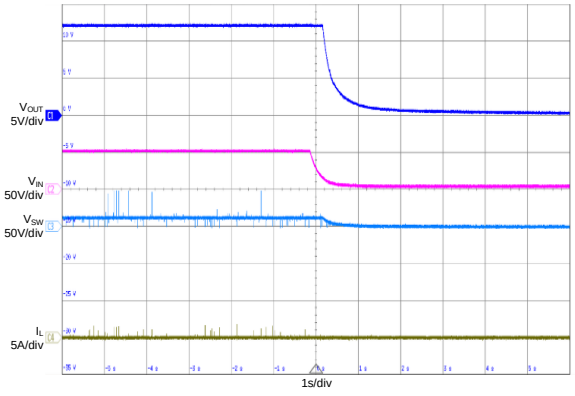


Figure 24. Shutdown through V_{IN} (I_{OUT} = 0A)

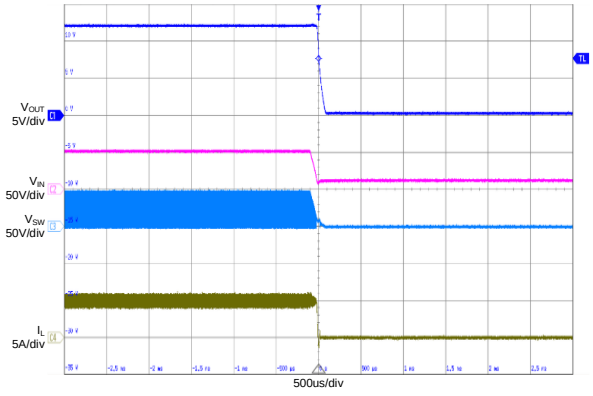


Figure 25. Shutdown through V_{IN} (I_{OUT} = 5A)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Non-Sync buck, f_{SW} = 500kHz, C_{IN} = 4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

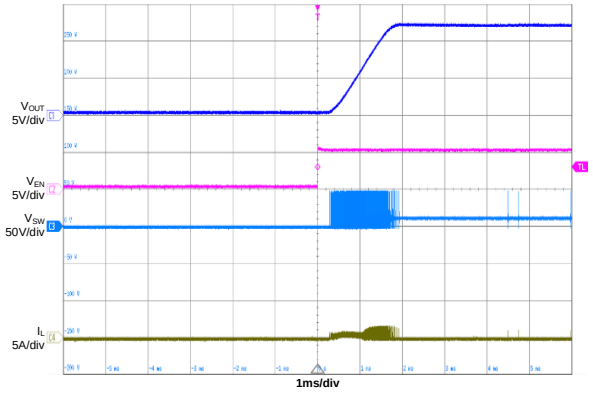


Figure 26. Startup through EN (I_{OUT} = 0A)

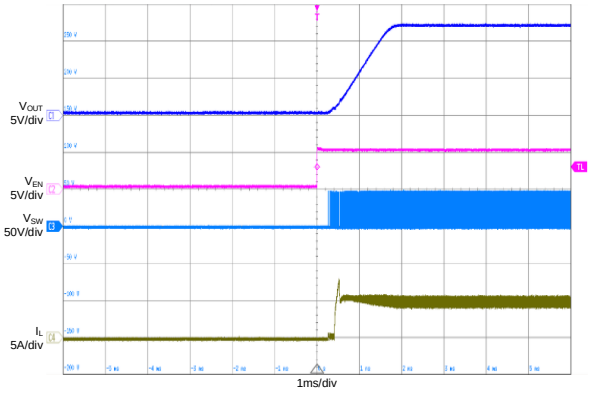


Figure 27. Startup through EN (I_{OUT} = 5A)

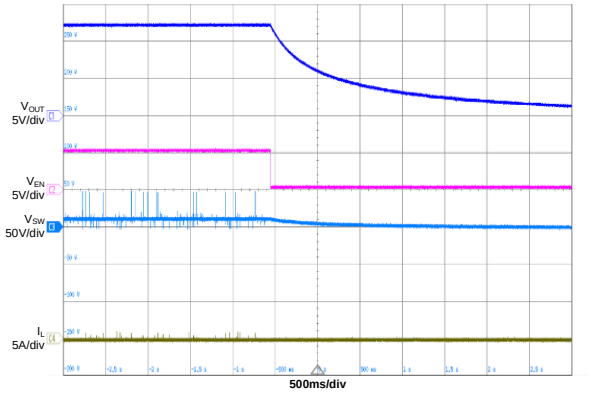


Figure 28. Shutdown through EN (I_{OUT} = 0A)

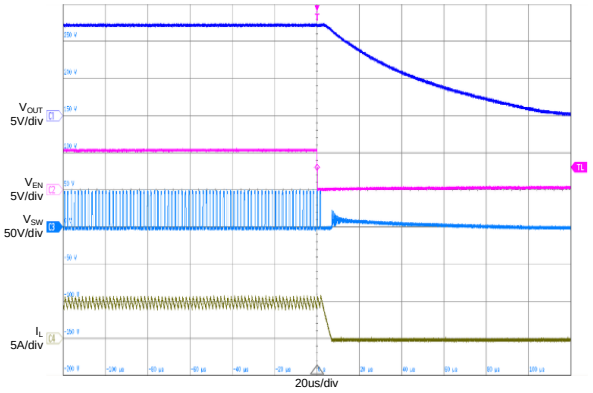


Figure 29. Shutdown through EN (I_{OUT} = 5A)

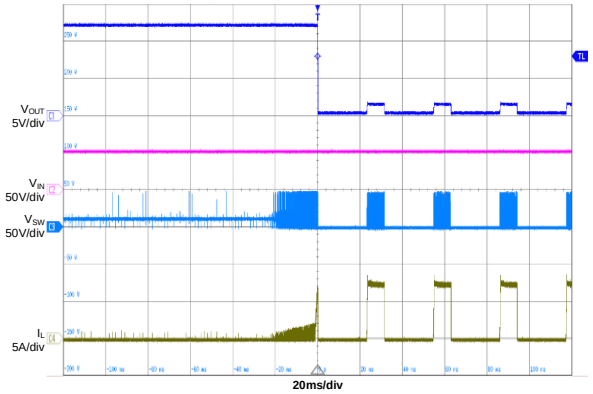


Figure 30. SCP Entry (I_{OUT} = 0A)

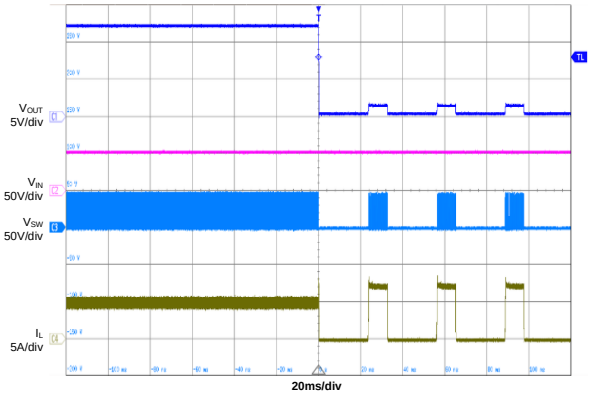


Figure 31. SCP Entry (I_{OUT} = 5A)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Non-Sync buck, f_{SW} = 500kHz, C_{IN} = 4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

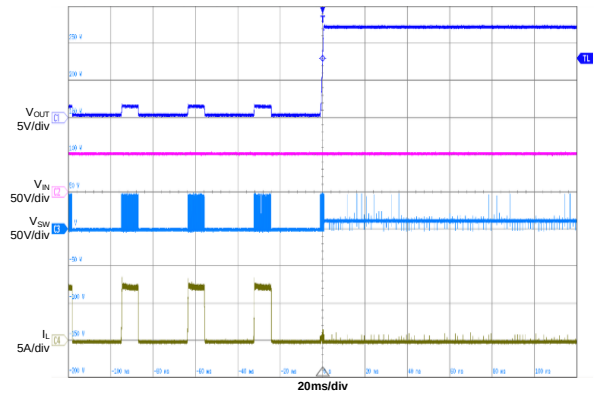


Figure 32. SCP Recovery (I_{OUT} = 0A)

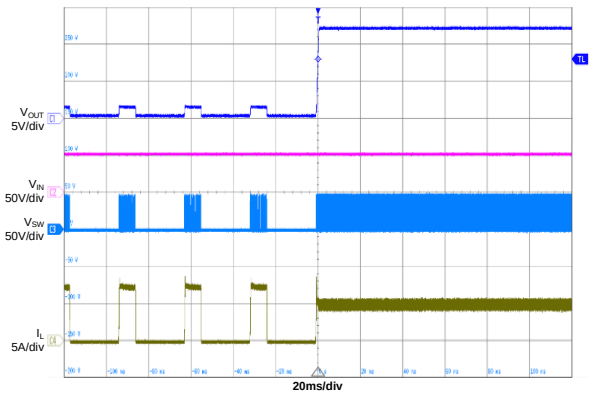


Figure 33. SCP Recovery (I_{OUT} = 5A)

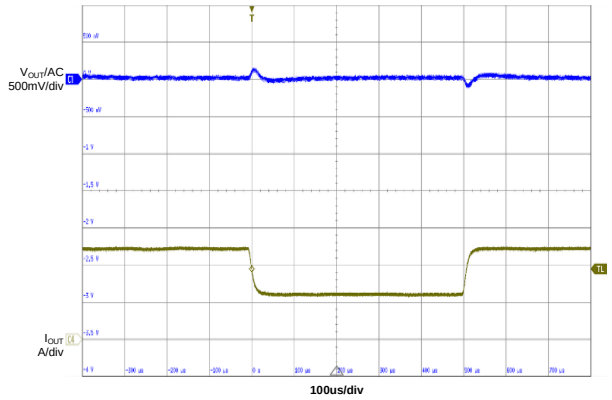


Figure 34. Load Transient (I_{OUT} = 2.5A to 5A, slew rate=3A/μs setting by E-load)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Sync buck, f_{SW} = 500kHz, C_{IN} =4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

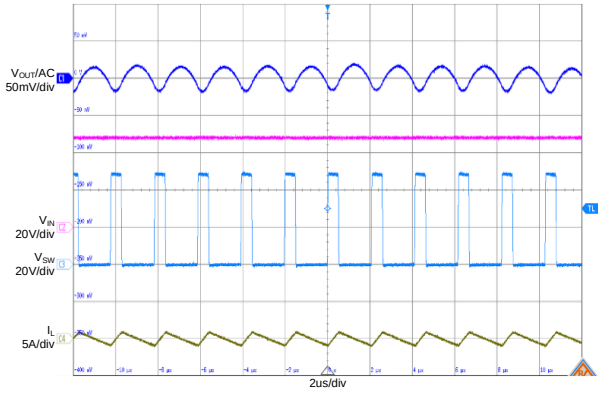


Figure 35. Output Voltage Ripple (I_{OUT} = 0A)

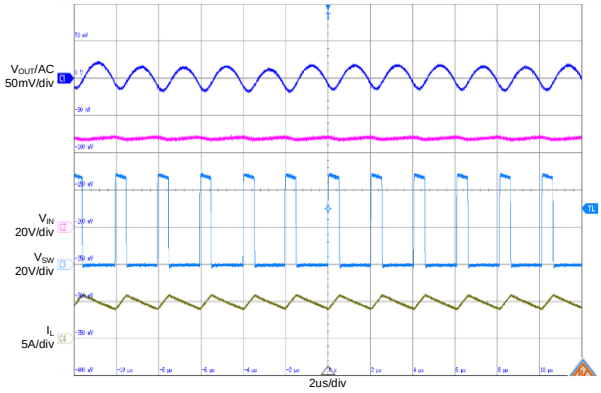


Figure 36. Output Voltage Ripple (I_{OUT} = 5A)

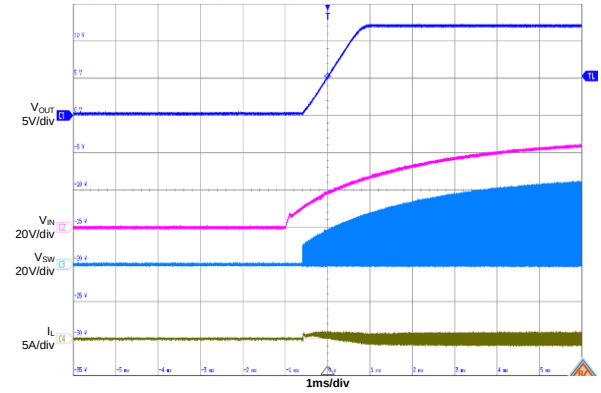


Figure 37. Startup through V_{IN} (I_{OUT} = 0A)

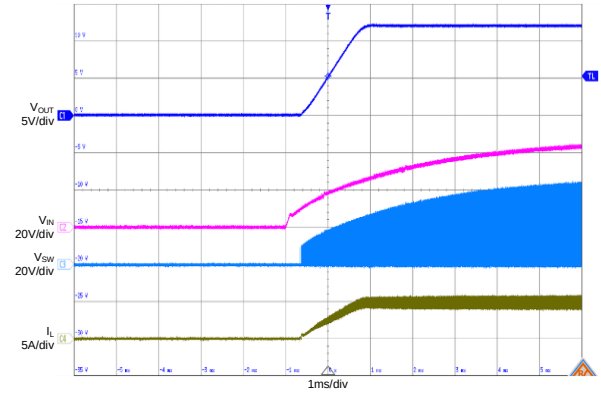


Figure 38. Startup through V_{IN} (I_{OUT} = 5A)

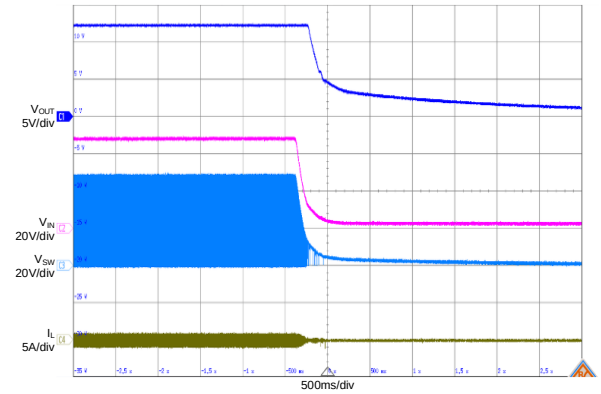


Figure 39. Shutdown through V_{IN} (I_{OUT} = 0A)

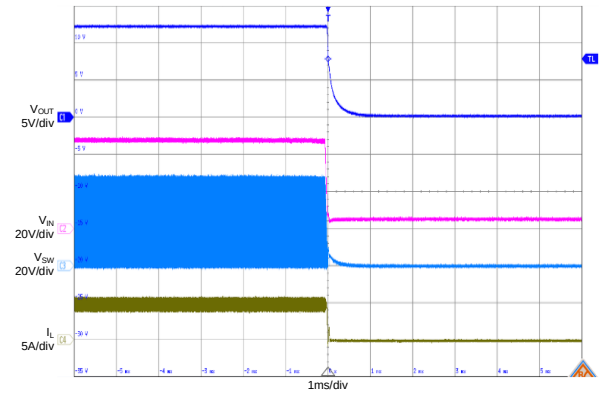


Figure 40. Shutdown through V_{IN} (I_{OUT} = 5A)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Sync buck, f_{SW} = 500kHz, C_{IN} =4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

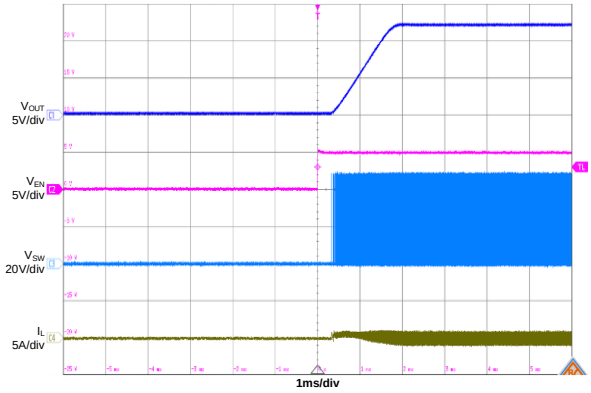


Figure 41. Startup through EN (I_{OUT} = 0A)

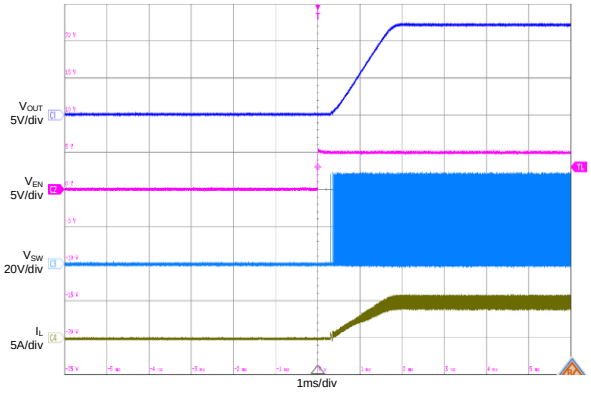


Figure 42. Startup through EN (I_{OUT} = 5A)

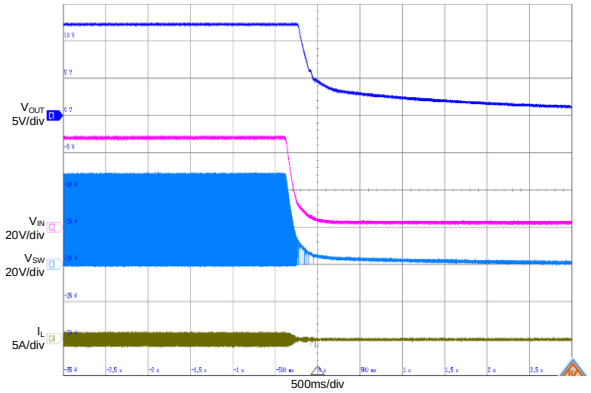


Figure 43. Shutdown through EN (I_{OUT} = 0A)

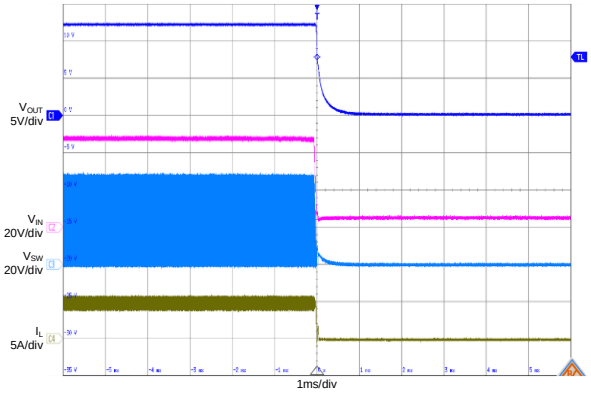


Figure 44. Shutdown through EN (I_{OUT} = 5A)

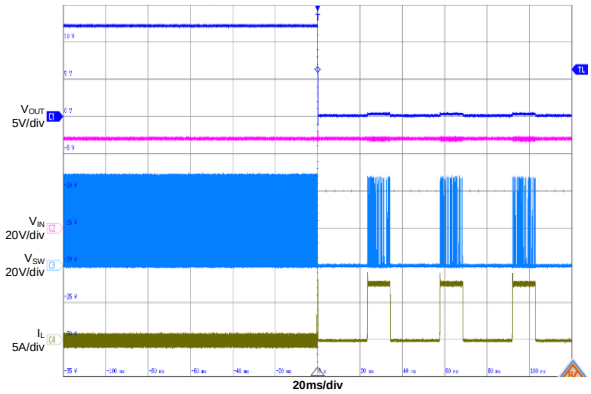


Figure 45. SCP Entry (I_{OUT} = 0A)

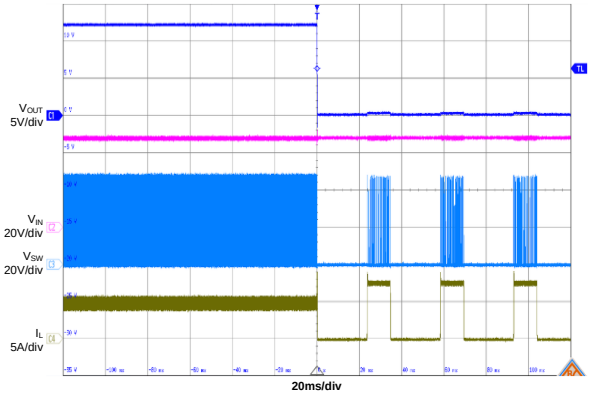


Figure 46. SCP Entry (I_{OUT} = 5A)

Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, Sync buck, f_{SW} = 500kHz, C_{IN} =4.7μF*2, C_{OUT} = 22μF*3, T_A = +25°C, unless otherwise noted.

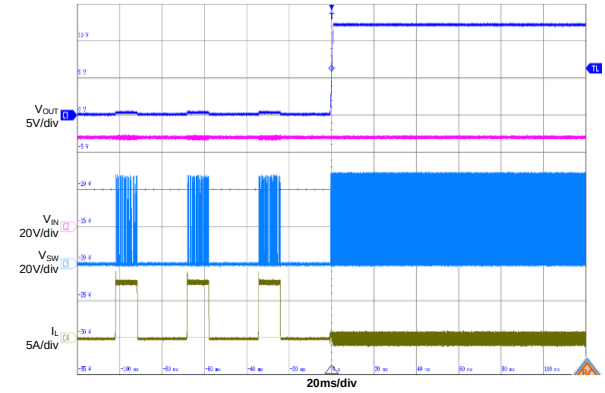


Figure 47. SCP Recovery (I_{OUT} = 0A)

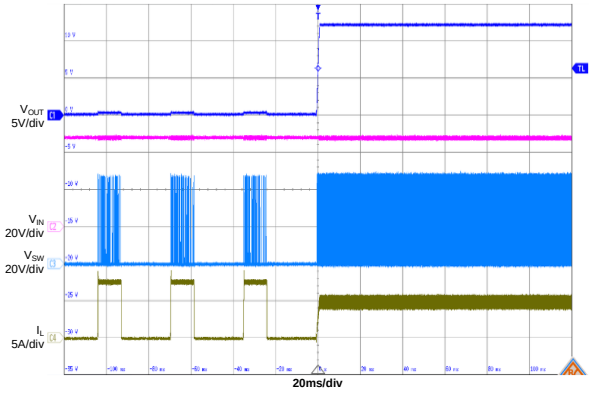


Figure 48. SCP Recovery (I_{OUT} = 5A)

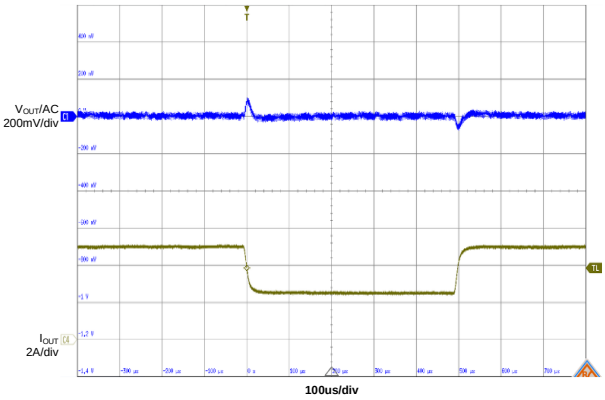


Figure 49. Load Transient (I_{OUT} = 2.5A to 5A, slew rate=3A/μs setting by E-load)

8 Layout Guidelines and Example

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

1) Place the input capacitor as close to VIN and GND as possible.
2) Place the external feedback resistors as close to FB as possible.
3) Keep the switching node (such as SW, BST) far away from the feedback network.
4) Minimize the power loop area formed by the input capacitor, IC, freewheeling diode or MOSFET, inductor and output capacitor.

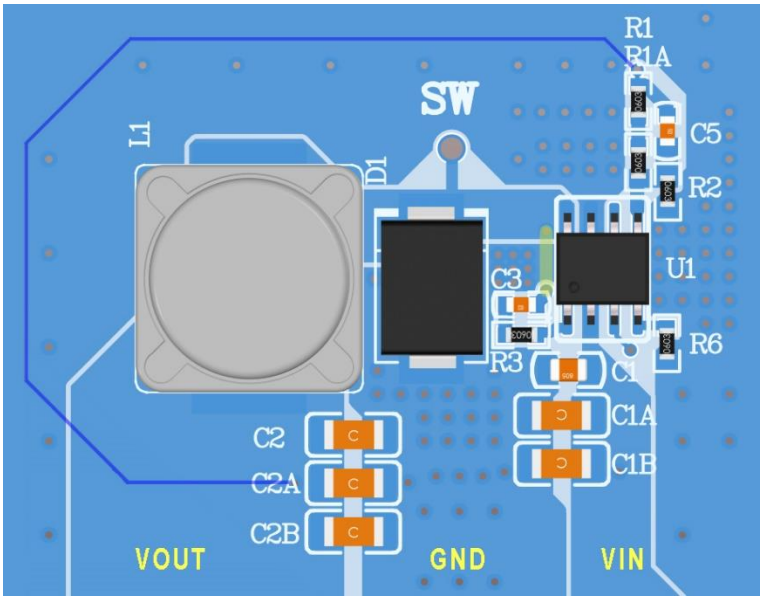


Figure 50. Recommend Non-Sync buck PCB Layout (Top Layer)

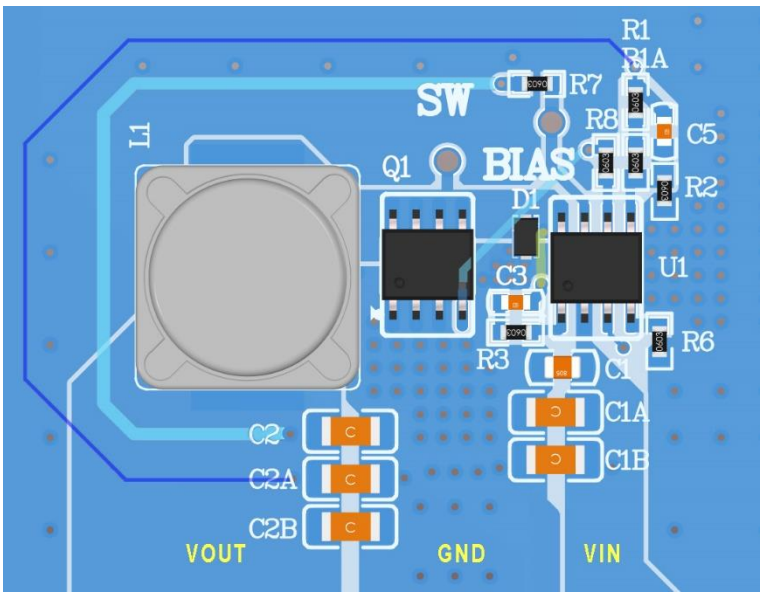
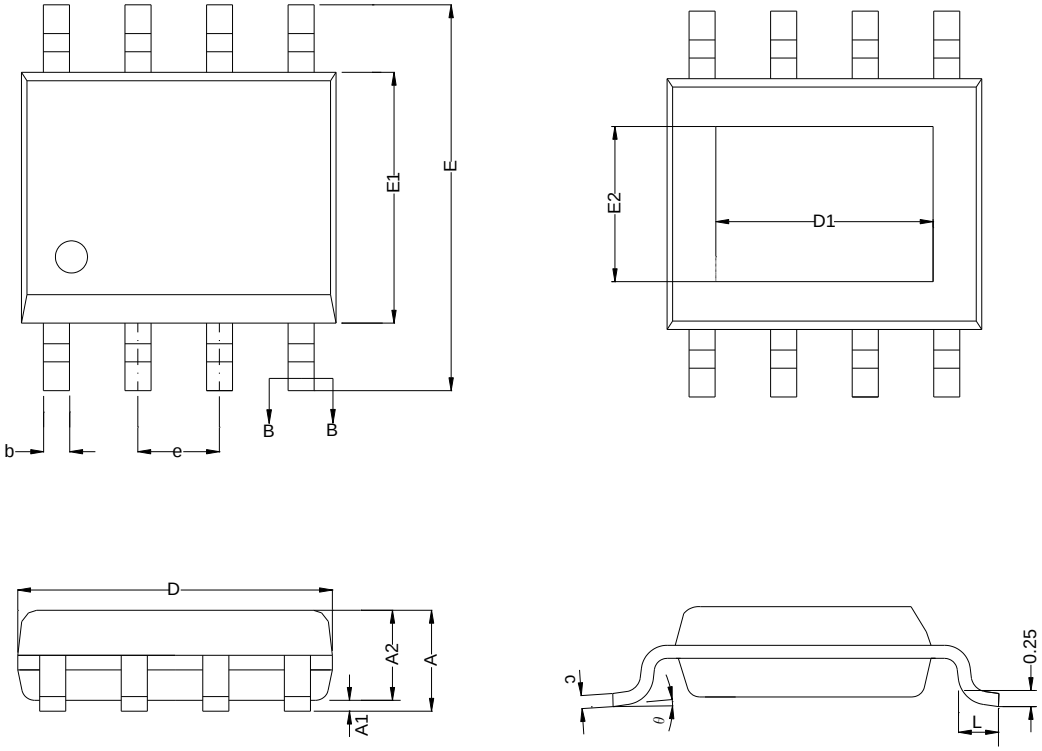


Figure 51. Recommend Sync buck PCB Layout (Top Layer)

9 Package Information

9.1 Outline Dimensions

ESOP8 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 4 *ESOP8 dimensions(mm)*.

Table 4. ESOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30		1.70
b	0.33		0.51
c	0.19		0.25
D	4.80	4.90	5.00
D1	3.15		3.45
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.26		2.56
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1602WGTR-I	ESOP8	Green	Tape & Reel	4000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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