70V, 3A, Asynchronous Step-down Converter

1 Features

- 4.5V to 70V Wide Operational Range
- Continuous Output Current: 3A
- Integrated High Side NMOS with180mΩ Low Resistance
- Constant-On-Time Control
- Power Good status Indication
- 250kHz/500kHz/1.2MHz Switching Frequency Selectable
- Valley Current Limiting for Non-Synchronous Buck Topology
- Low Quiescent Current: 150μA
- Low Shutdown Current: 3μA
- Built-in Pull-up Current at EN Pin
- Low Drop Out Mode Support 98% Duty Cycle
- Available in ESOP8 Package

2 Applications

- 12V, 24V and 48V Power Systems
- Surveillance Camera
- PoE Switch
- Industry applications

3 Description

The GD30DC1601-I is a 70V, 3A step-down converter which is Integrated high-side power MOSFET with 180mΩ low resistance. Featuring constant on-time (COT) control, the GD30DC1601-I efficiently delivers up to 3A of output current while ensuring a rapid loop response.

This device optimizes power conversion efficiency across various load conditions by reducing its switching frequency during light loads. This approach minimizes both switching and gate driving losses.

Equipped with essential protection mechanisms, the GD30DC1601-I includes a cycle-by-cycle current limit, short-circuit protection with hiccup mode, FB open protection, and thermal shutdown.

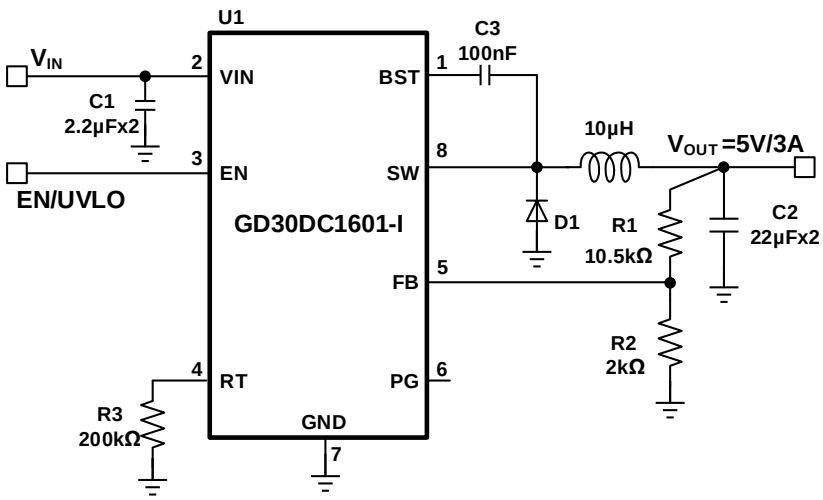
The GD30DC1601-I is available with space saving ESOP8 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1601-I	ESOP8	4.90 mm x 3.90 mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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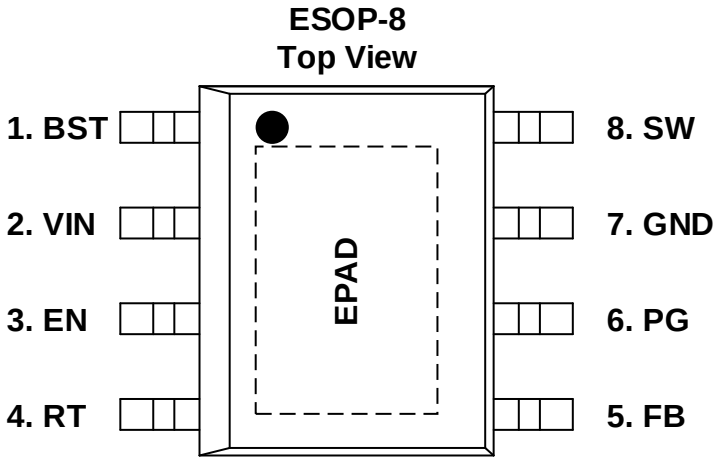
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	ESOP8		
BST	1	O	**Bootstrap**. Connect a high-quality BST capacitor between SW and BST to form a floating supply across the high-side switch driver.
VIN	2	P	**Power supply**. Operates from a 4.5V to 70V input rail. Supply input terminal to internal bias LDO and high-side FET. A decoupling capacitor is required to decouple the input.
EN	3	I	**Enable**. Pull high to enable the output. It is internally pulled up via a current source.
RT	4	I	**Frequency Set Pin.** Attach a resistor between the RT pin and GND to set the switching frequency. Selectable options include 250kHz, 500kHz, and 1.2MHz.
FB	5	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider from VOUT to GND.
PG	6	O	**Power Good Indication.** Open-drain structure, needs to be connected to an external voltage source through a pull-up resistor.
GND	7	G	**Ground Pin.** Chip's GND connection. Connect to the ground of the system.
SW	8	O	**Switch output**. Switching node of power stage. Connected to the internal MOSFET switches and inductor terminal.
EPAD	9	G	**Exposed Pad.** Connect the exposed pad to the PCB GND plane to ensure optimal thermal efficiency.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	VIN to GND	−0.3	72	V
V_{EN}	EN to GND	−0.3	72	V
V_{SW}	SW to GND	−0.6	V_{IN}+0.3	V
V_{BST-SW}	BST to SW	−0.3	6	V
All Other Pins		−0.3	6	V
T_{STG}	Storage temperature	−55	150	°C
T_J	Junction temperature	-40	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	VIN to GND	4.5		70	V
V_{OUT}	VOUT to GND	0.8		40	V
I_{OUT}	Max Continuous Output Current			3	A
T_J	Junction temperature	−40		125	°C

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	ESOP8	48	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	ESOP8	52	°C/W
$\Theta_{JC(BOT)}$	Junction to case (bottom) thermal resistance	ESOP8	2.3	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN}=48V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO and QUIESCENT CURRENT						
VIN_{UV_R}	VIN UVLO rising threshold			4.25		V
VIN_{UV_F}	VIN UVLO falling voltage			4		V
VIN_{UV_HYS}	Hysteresis voltage of VIN UVLO			0.25		V
I_Q	Quiescent current	V_{FB} = 0.85V		150		μA
I_S	Shutdown current	V_{EN} = 0V		3		μA
ENABLE						
V_{EN_R}	EN rising threshold			1.2		V
V_{EN_F}	EN falling threshold			0.95		V
$I_{EN\_PULL\_UP}$	EN pulled up current	EN = L		1		μA
		EN = H		4		
I_{EN_HYS}	EN pulled up current hysteresis			3		μA
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage		0.788	0.8	0.812	V
V_{FB_UV}	FB UV threshold			0.1		V
POWER STAGE						
R_{HS_ON}	HS on resistance	V_{BST}-V_{SW} = 5V		180		mΩ
I_{LKG_HS}	HS leakage current	V_{EN} = 0V, V_{SW} = 0V			1	μA
CURRENT LIMIT						
I_{LIMIT_HS}	High side current limit threshold			5.9		A
SOFT START						
T_{SS}	Internal Soft-start time	V_{FB} from 10% to 90%		2		ms
SWITCHING FREQUENCY FUNCTION						
F_{SW}	Switching Frequency	RT Pin float		250		kHz
		R_{RT} = 200kΩ		500		kHz
		R_{RT} = 80kΩ		1200		kHz
T_{ON_MIN}	Min On pulse			150		ns
T_{ON_MAX}	Max On pulse			20		μs
T_{OFF_MIN}	Min Off time			350		ns
POWER GOOD						
$V_{PG\_UV\_F}$	FB threshold for PG low	FB falling		90		%
$V_{PG\_OV\_R}$	FB threshold for PG low	FB rising		108		%
R_{PG_ON}	PG on resistance	Sink 3mA		6		Ω
T_{PG_DELAY}	PG delay time	L to H and H to L		50		μs

Electrical Characteristics (continued)

V_{IN}=48V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL PROTECTION						
T_{OTP_R}[1]	Over temperature protection rising threshold			160		°C
T_{OTP_F}[1]	Over temperature protection falling threshold			140		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

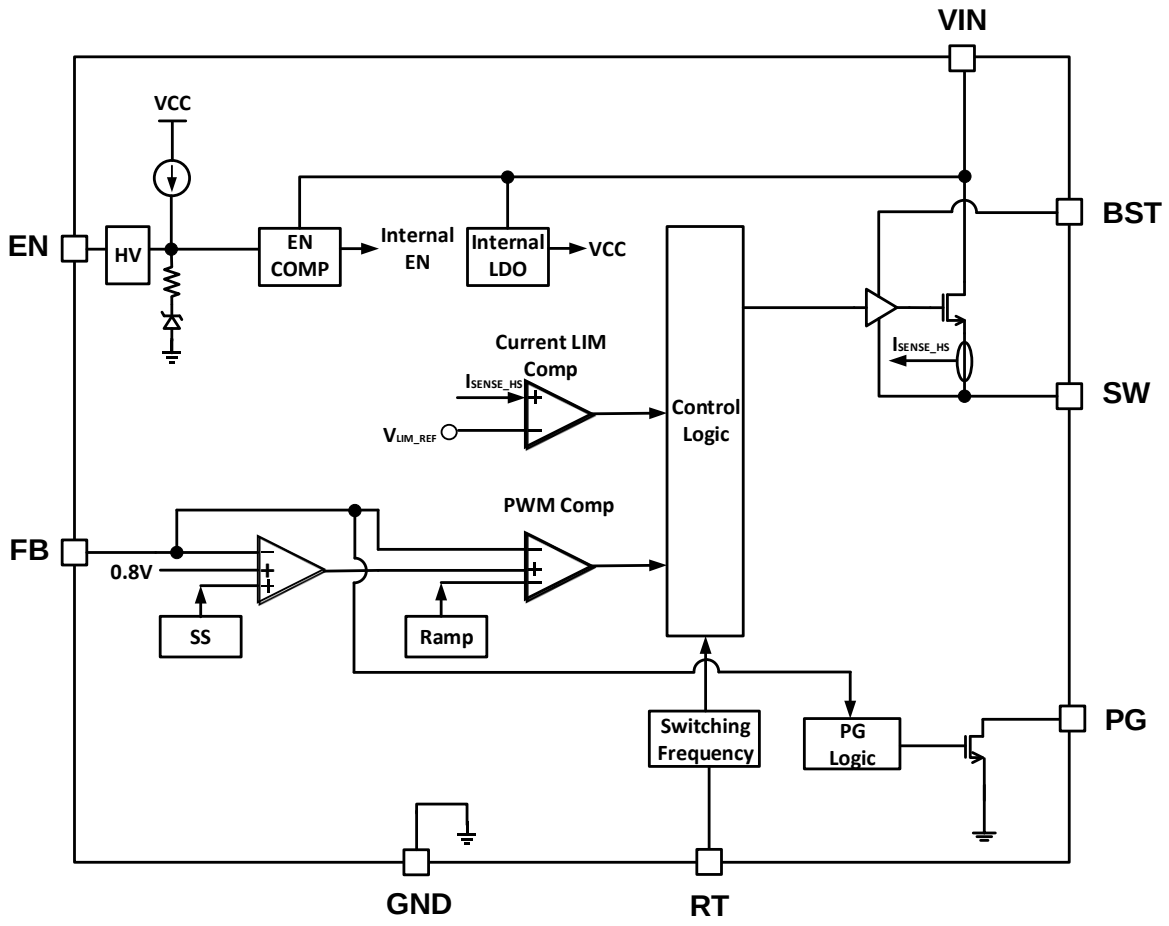


Figure 1. GD30DC1601-I Functional Block Diagram

6.2 Operation

6.2.1 Pulse-Width Modulation (PWM) Operation

The GD30DC1601-I is a fully integrated non-synchronous step-down converter. It utilizes constant-on-time (COT) control to achieve fast transient response and simplify loop stabilization. At the start of each cycle, the high-side MOSFET (HS-FET) is activated when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), signaling that the output voltage is insufficient. The on-time duration is determined by both the input and output voltages, ensuring relatively stable switching frequency across the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. Through this repetitive process, the converter regulates the output voltage.

To enhance stability, internal compensation is integrated with the COT control, enabling stable performance even when ceramic capacitors are used for output. This internal mechanism also improves jitter performance without affecting the line or load regulation.

6.2.2 Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current remains above zero amps (see Figure 2). When the V_{FB} falls below the V_{REF}, the HS-FET turns on for a fixed duration controlled by the one-shot timer. Once the HS-FET switches off, the external free-wheeling diode carries the current.

In CCM, the switching frequency remains relatively stable, a behavior known as pulse-width modulation (PWM) mode.

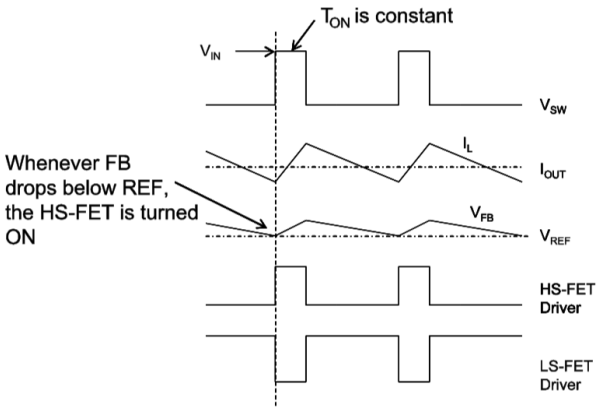


Figure 2. Heavy-Load Operation

6.2.3 Light-Load Operation

In a non-synchronous application, a diode is used. As the load decreases, the inductor current also drops. When the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load behavior is illustrated in Figure 3. When theV_{FB} falls below the V_{REF}, the HS-FET turns on for a fixed duration determined by the one-shot timer. After the HS-FET turns off, the free-wheeling diode activates until the inductor current hits zero. In DCM, V_{FB} cannot reach V_{REF} while the inductor current approaches zero. At this point, the free-wheeling diode blocks any negative current, and the IC enters a tri-state mode. The output capacitor slowly discharges to GND via the feedback resistor, significantly enhancing efficiency during light-load conditions.In light-load mode, the HS-FET activates less frequently compared to heavy-load conditions, a behavior known as skip mode.

At light or no load, the output drops very slowly, and the GD30DC1601-I naturally lowers its switching frequency, thereby achieving high efficiency during light loads.

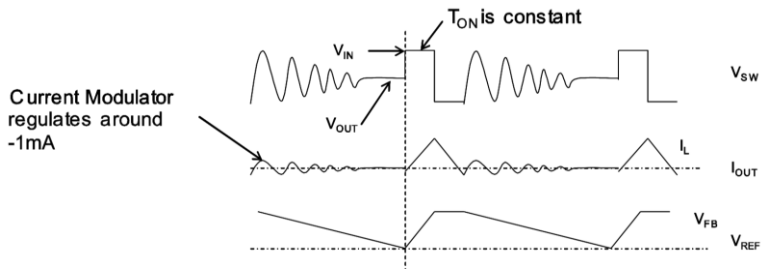


Figure 3. Light-Load Operation

As the output current rises from a light-load state, the regulation period of the current modulator becomes shorter. The HS-FET is activated more frequently, leading to an increase in the switching frequency. When the modulation time reduces to zero, the output current reaches the critical level. The critical output current can be calculated using the equation provided below.

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device switches to PWM mode once the output current surpasses the critical level. Afterward, the switching frequency remains relatively stable across the output current range.

6.2.4 Under-Voltage Lockout (UVLO) and Enable (EN) Control

The under-voltage lockout (UVLO) feature ensures the chip does not operate at inadequate supply voltages. The GD30DC1601-I UVLO comparator monitors the input voltage, with a rising threshold of approximately 4.25V and a falling threshold of 4V.

The GD30DC1601-I includes a dedicated enable control pin with positive logic. To activate the regulator, apply a voltage above 1.2V (typical) to the EN pin, and to disable it, set the EN pin voltage below 0.95V (typical). By using two external resistor dividers, the start and stop voltages of the system can be easily optimized via the EN pin.

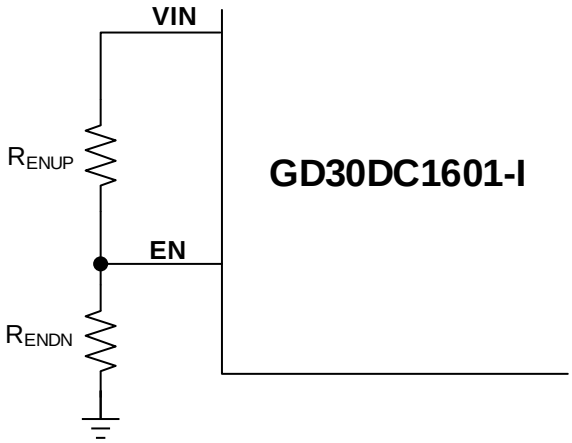


Figure 4. EN divider for adjustable UVLO

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 0.95 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (3)$$

6.2.5 Internal Soft Start (SS)

The soft-start (SS) function prevents output voltage overshoot during start-up. When the chip powers on, the internal circuit generates a soft-start voltage (V_{SS}) that gradually increases from 0V to 1V. While V_{SS} remains below V_{REF}, V_{SS} replaces V_{REF} as the reference for the error amplifier. Once V_{SS} surpasses V_{REF}, the error amplifier switches back to using V_{REF}. The soft-start duration is internally set to 2ms (from 10% to 90%).

6.2.6 Switching Frequency Set

The RT pin allows configuration of the switching frequency, with three available options for the GD30DC1601-I: 250kHz, 500kHz, and 1200kHz. The desired frequency is set by selecting the appropriate resistor value connected between RT and GND. Refer to the table below for details.

Table 1. Switching frequency set resistor selection

RT Resistor	Switching Frequency
Float	250 kHz
200 kΩ (±20%) to GND/ short to GND	500 kHz
80 kΩ (±20%) to GND	1200 kHz

6.2.7 High Duty Mode Operation

GD30DC1601-I will automatically extend the on time to support the application when V_{IN} is close to V_{OUT}. The on time extend circuit will be triggered when T_{OFF_MIN} time is reached. The GD30DC1601-I can support up to 98% maximum duty cycle at 250 kHz and 500 kHz. The GD30DC1601-I can support up to 57% maximum duty cycle at 1200 kHz.

6.2.8 Current Limit and Short Protection

The GD30DC1601-I features both a peak current limit and a unique valley current limit. While the HS-FET is on, the inductor current is monitored. If the sensed inductor current exceeds the peak current limit after the blanking time, the HS-FET turns off. However, in a non-synchronous buck configuration, the inductor current might increase uncontrollably during output short-circuit conditions due to the blanking time. The GD30DC1601-I utilizes a special valley current limit to prevent this issue. When the HS-FET is off and the inductor current exceeds the valley current limit, the HS-FET remains off until the output current falls below the valley current limit threshold.

In cases where the output is shorted to ground, the GD30DC1601-I automatically reduces the switching frequency to prevent current runaway, enhancing system reliability.

6.2.9 Power Good Indication

The GD30DC1601-I includes a power good (PG) indicator function, implemented via an open-drain output. When the output voltage reaches its target level, the internal PG pull-down circuitry is disabled, and the PG signal is pulled high by V_{CC} or an external voltage source. When the output voltage drops below 90% or rises above 108% of the target value, the PG signal is pulled down internally. A resistor with a value between 10kΩ and 100kΩ is recommended between PG and V_{CC}.

If the input supply fails to power the GD30DC1601-I, the PG signal remains clamped low even if PG is connected to an external DC source through a pull-up resistor. The relationship between PG voltage and PG sink current is illustrated in Figure 5 below:

If the input supply fails to power the GD30DC1601-I, PG is clamped low even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the PG sink current is shown in Figure 5 below:

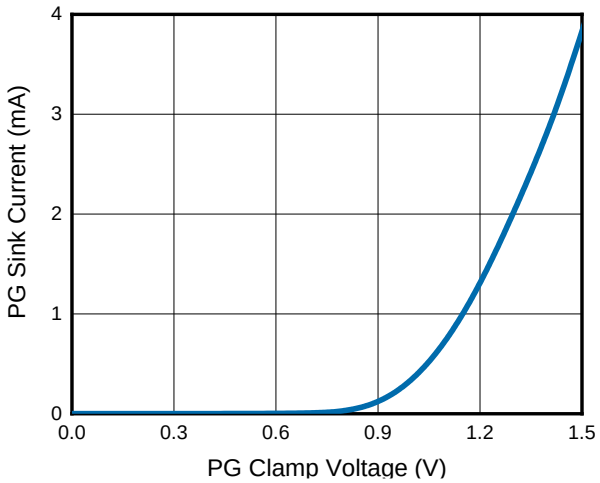


Figure 5. PG sink current VS. PG clamped voltage

6.2.10 Thermal Shutdown

The thermal shutdown feature protects the chip from excessive temperatures. If the silicon die temperature exceeds 160°C, the chip automatically powers down. It reactivates once the temperature drops below the lower threshold, typically 140°C.

7 Application Information

7.1 Typical Application Circuit

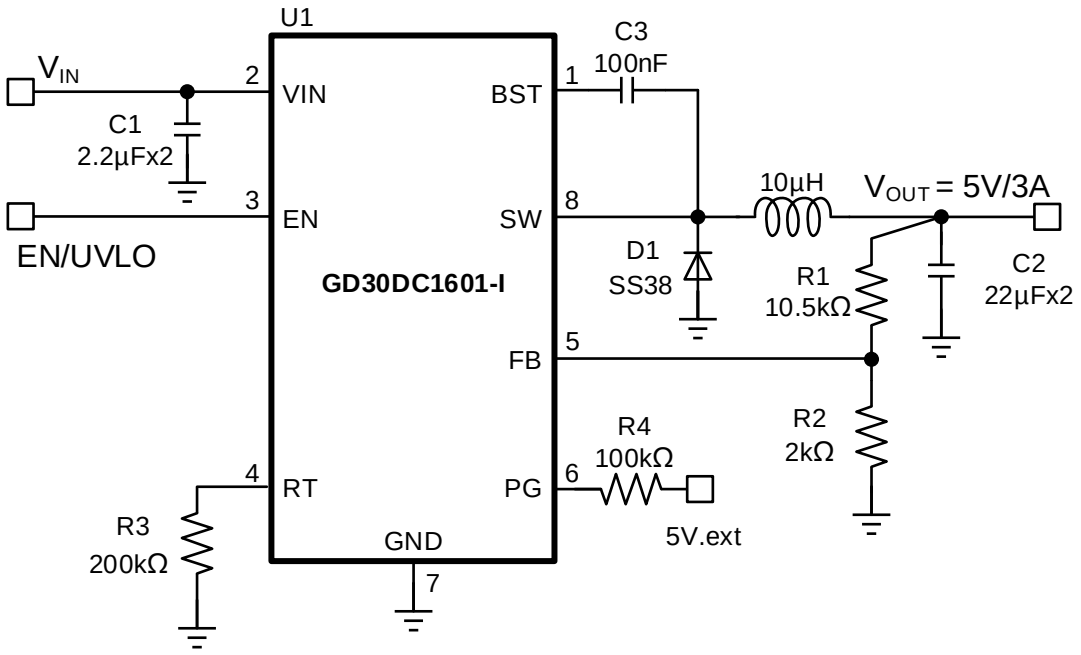


Figure 6. V_{IN}=48V, V_{OUT}=5V/3A, F_{SW}=500kHz

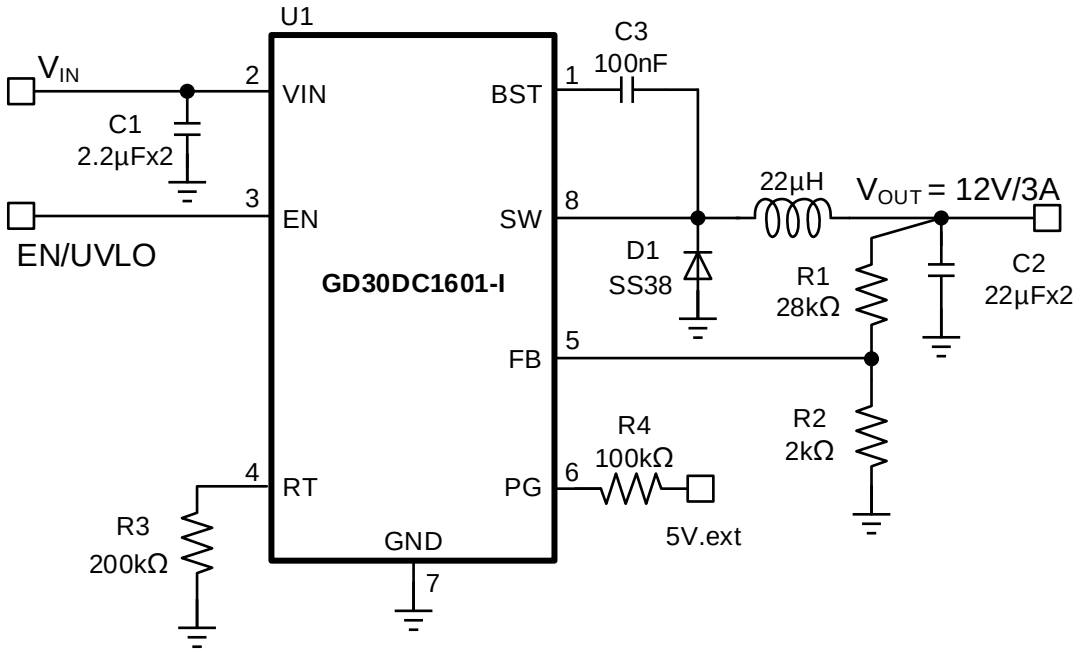


Figure 7. V_{IN}=48V, V_{OUT}=12V/3A, F_{SW}=500kHz

7.2 Detailed Design Description

7.2.1 Setting the Output Voltage

The GD30DC1601-I output voltage is configured via external resistor dividers, with a fixed reference voltage of 0.8V. The feedback network layout is shown in the figure below.

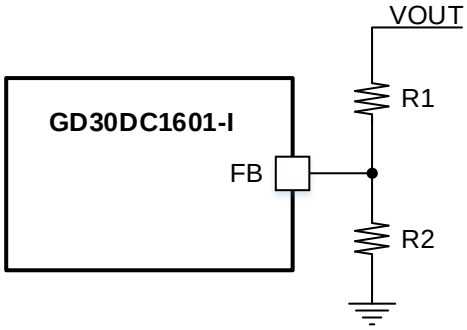


Figure 8. Feedback resistor divider

Choose R1 and R2 using Equation(4):

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \quad (4)$$

7.2.2 Selecting the Inductor

An inductor is essential for providing continuous current to the load while being driven by the switched input voltage. A larger inductor minimizes ripple current and reduces output voltage ripple but comes with drawbacks such as a larger physical size, higher series resistance, and lower saturation current. For most designs, the suitable inductance value can be calculated using the following Equation(5):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (5)$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation(6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2. Resistor Selection for Common Output Voltages[1]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{ff} (pF)	L(μH)	RT(kΩ)	C_{OUT}(μF)
12	28	2	33 (optional)	22	200	44
5	10.5	2	100 (optional)	10	200	44

1. For a detailed design circuit, please refer to the Typical Application Circuits

7.2.3 Selecting the Output Capacitor

The output capacitor (C2) is responsible for maintaining the DC output voltage ripple. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred for minimizing output voltage ripple, which can be estimated using the Equation(7):

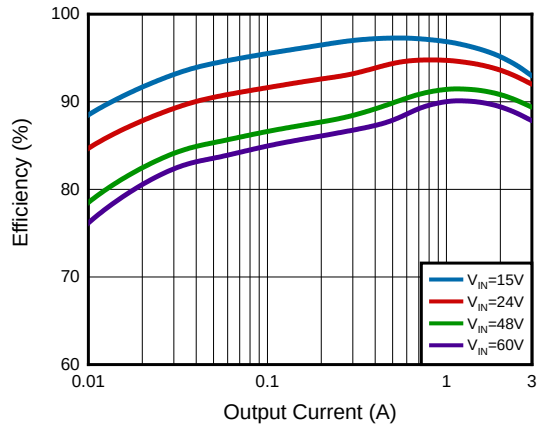
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also influence the stability of the regulation system. The GD30DC1601-I is designed to operate efficiently across a wide range of capacitance and ESR values.

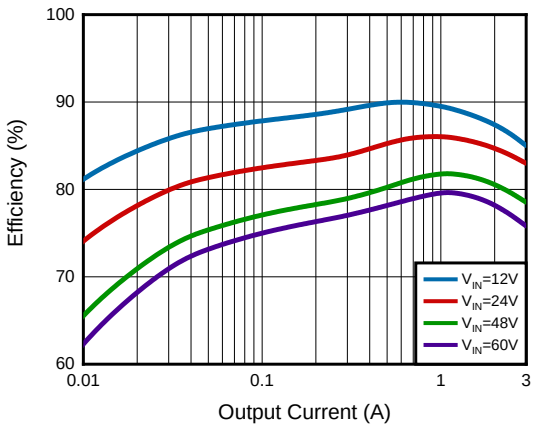
7.3 Typical Application Curves

V_{IN}=48V, V_{OUT}=12V, F_{SW}=500kHz, C_{IN}=4.7μF, C_{OUT}=2x22μF, L1=22μH, and T_A=+25°C, unless otherwise noted.



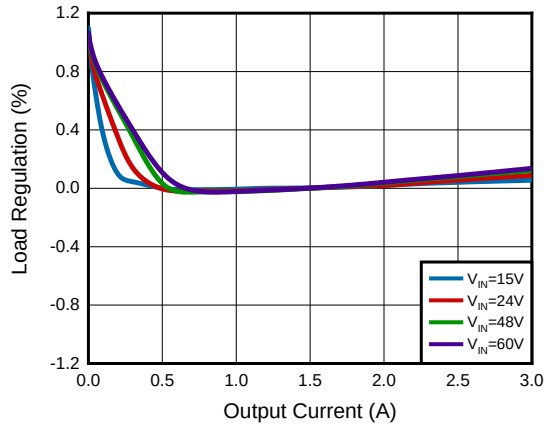
V_{OUT} = 12V, L1 = 22uH, DCR = 43mΩ

Figure 9. Efficiency vs. Load Current



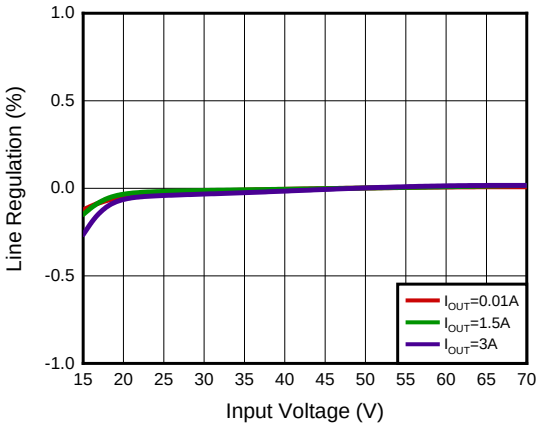
V_{OUT} = 5V, L1 = 10uH, DCR = 30mΩ

Figure 10. Efficiency vs. Load Current



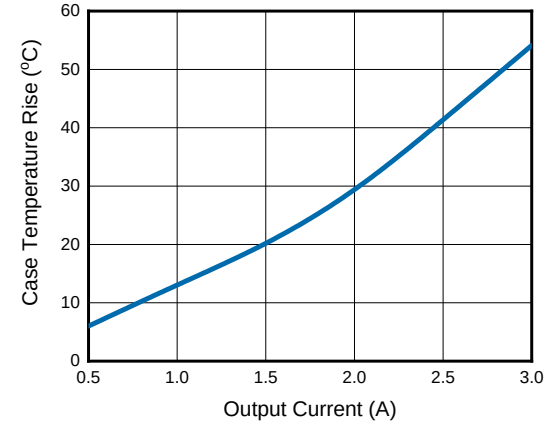
V_{OUT} = 12V, DCR = 43mΩ

Figure 11. Load Regulation



V_{OUT} = 12V, DCR = 43mΩ

Figure 12. Line Regulation

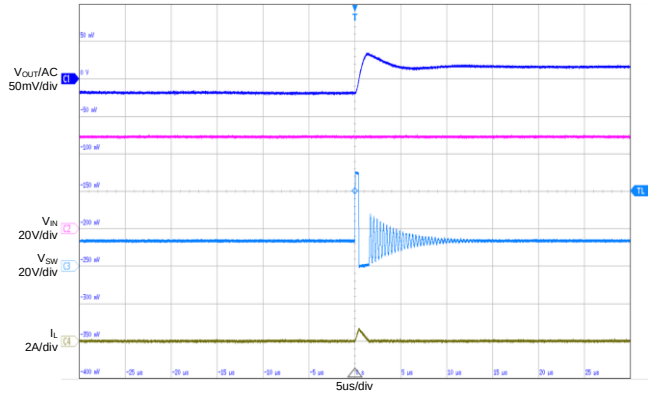


No air flow

Figure 13. Temperature Rise

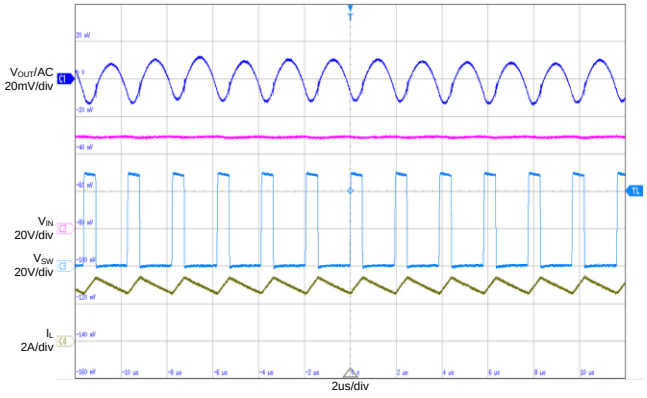
Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} =4.7μF, C_{OUT} =22μF*2, L1 = 22μH, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



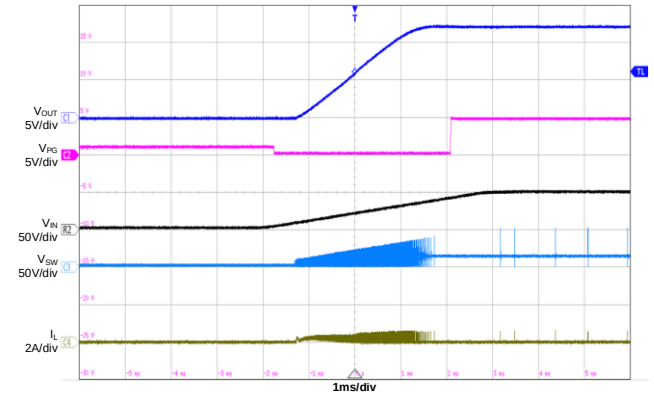
I_{OUT} = 0A

Figure 14. Output Voltage Ripple (I_{OUT}=0A)



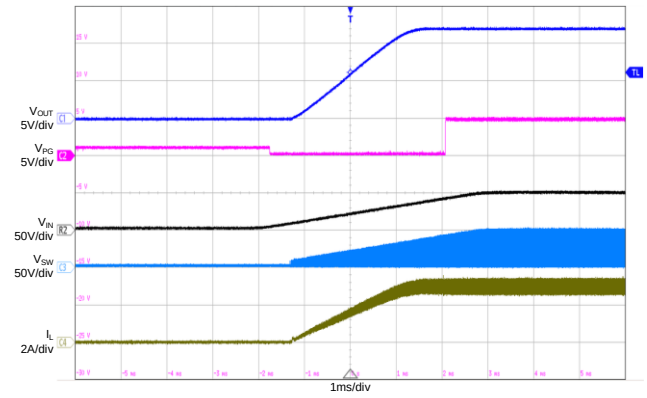
I_{OUT} = 3A

Figure 15. Output Voltage Ripple (I_{OUT}=3A)



I_{OUT} = 0A

Figure 16. Startup through V_{IN}

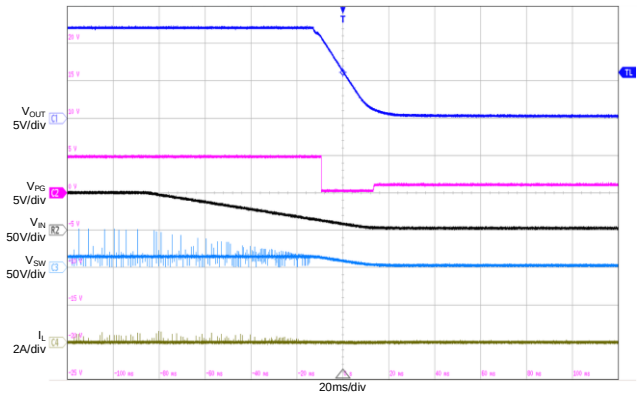


I_{OUT} = 3A

Figure 17. Startup through V_{IN}

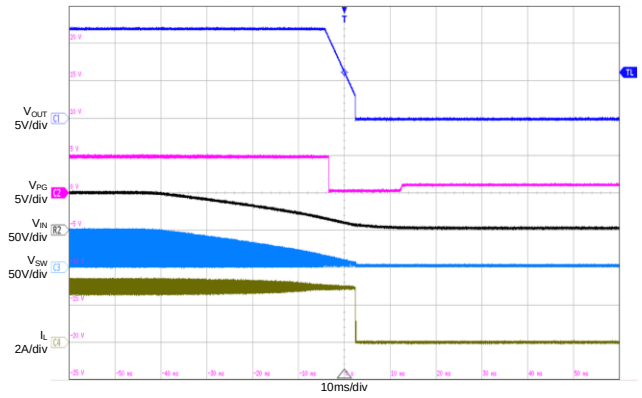
Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} =4.7μF, C_{OUT} =22μF*2, L1 = 22μH, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



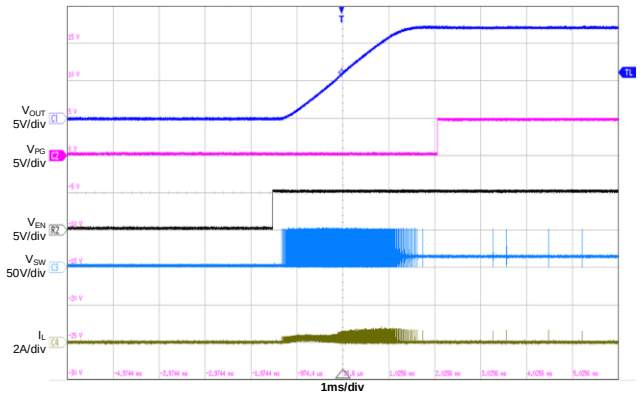
I_{OUT} = 0A

Figure 18. Shutdown through V_{IN}



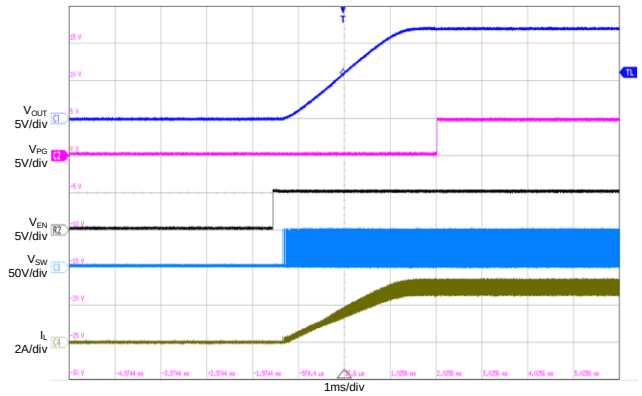
I_{OUT} = 3A

Figure 19. Shutdown through V_{IN}



I_{OUT} = 0A

Figure 20. Startup through EN

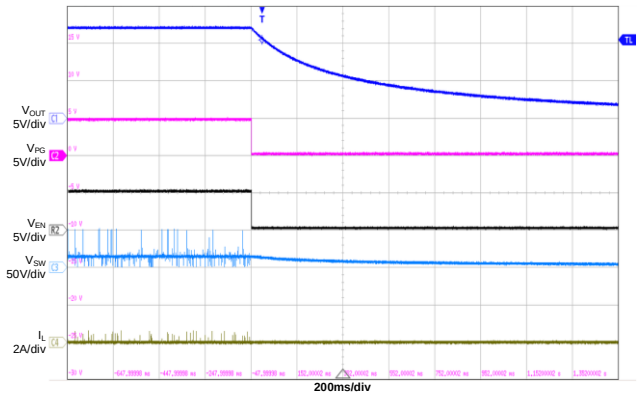


I_{OUT} = 3A

Figure 21. Startup through EN

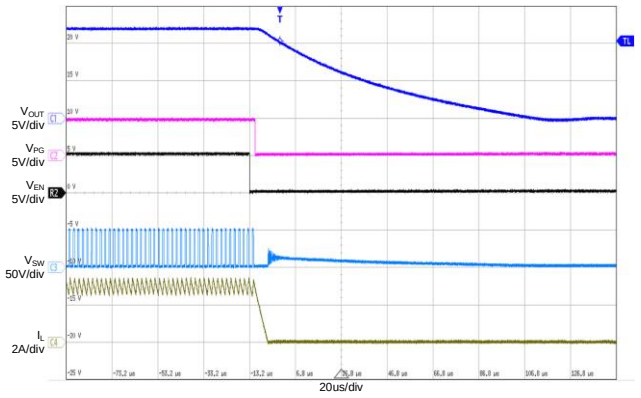
Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} =4.7μF, C_{OUT} =22μF*2, L1 = 22μH, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



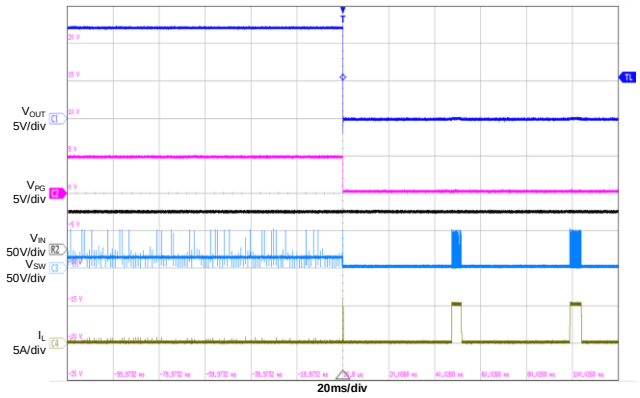
I_{OUT} = 0A

Figure 22. Shutdown through EN



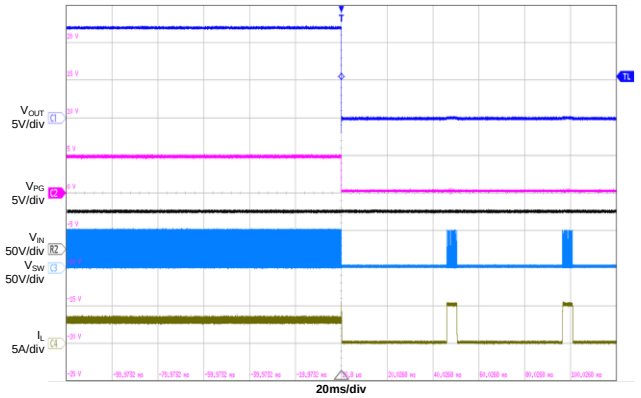
I_{OUT} = 3A

Figure 23. Shutdown through EN



I_{OUT} = 0A

Figure 24. SCP Entry

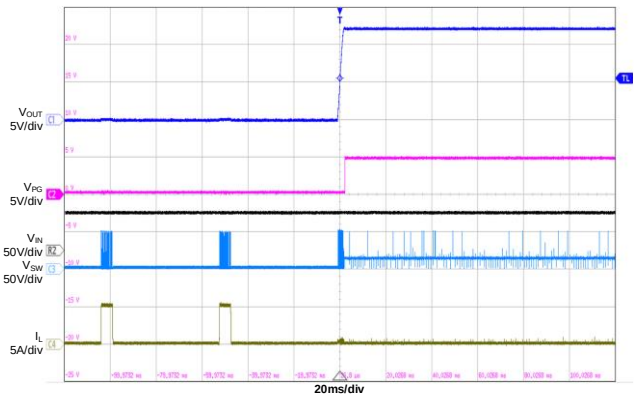


I_{OUT} = 3A

Figure 25. SCP Entry

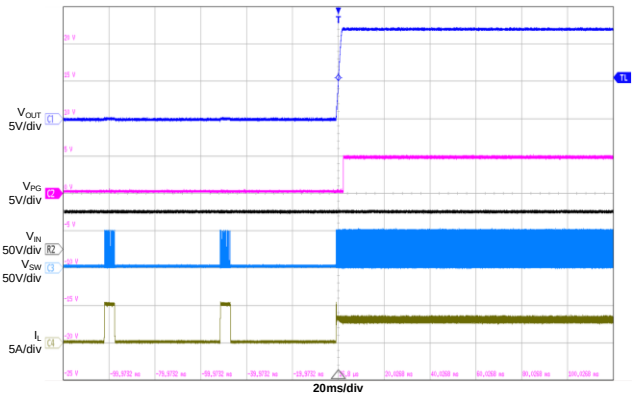
Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 500kHz, C_{IN} =4.7μF, C_{OUT} =22μF*2, L1 = 22μH, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



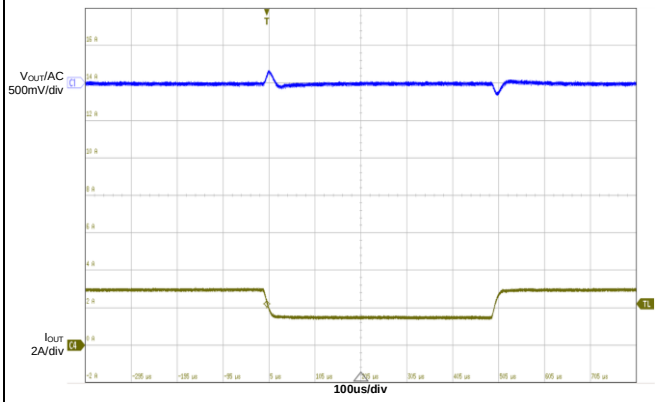
I_{OUT} = 0A

Figure 26. SCP Recovery



I_{OUT} = 3A

Figure 27. SCP Recovery



I_{OUT} = 1.5A to 3A, Slew Rate = 3A/μs

Figure 28. Load Transient

8 Layout Guidelines and Example

Proper layout design is essential for ensuring stable operation of switching power supplies. Poor layout in high-frequency switching converters can lead to instability and weak line or load regulation. For optimal performance, refer to the figure below and adhere to the following guidelines:

Position the input capacitor as close as possible to V_{IN} and GND.

Place the external feedback resistors near the FB pin for best accuracy.

Keep the switching nodes (e.g., SW and BST) away from the feedback network to reduce interference.

Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.

Add a grid of thermal vias beneath the exposed pad to enhance thermal conductivity.

1) Position the input capacitor as close as possible to VIN and GND.
2) Place the external feedback resistors as close to FB as possible.
3) Keep the switching nodes (e.g., SW and BST) away from the feedback network to reduce interference.
4) Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
5) Add a grid of thermal vias beneath the exposed pad to enhance thermal conductivity.

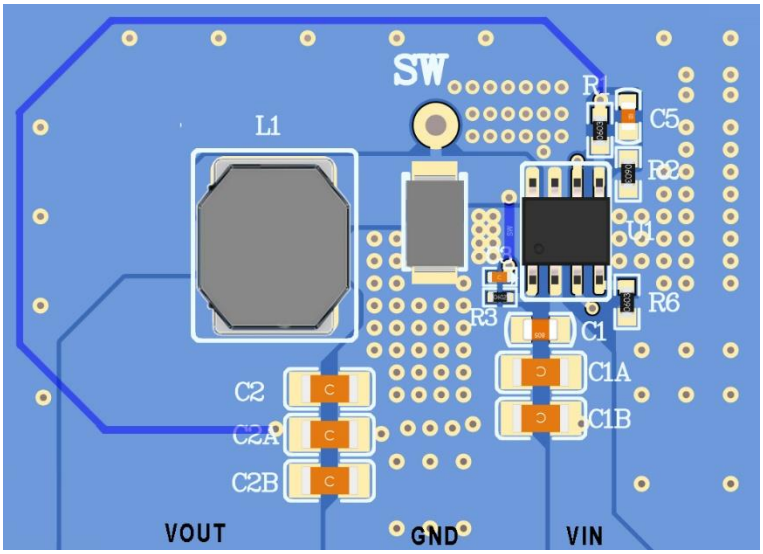
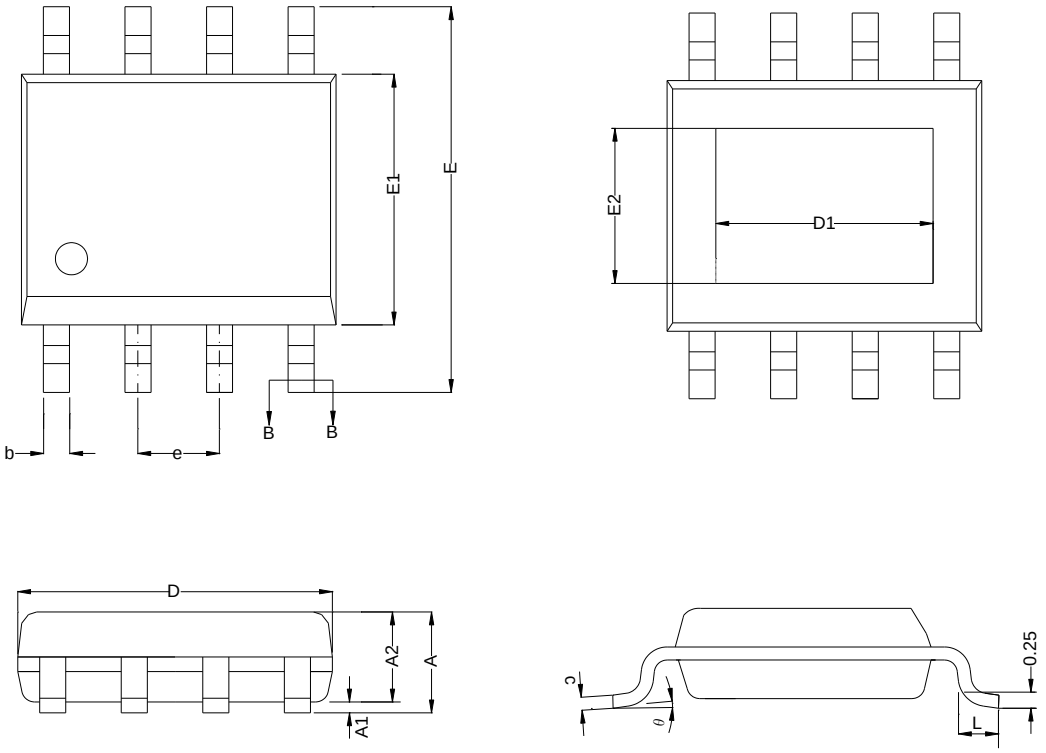


Figure 29. Typical GD30DC1601-I Example Layout

9 Package Information

ESOP8 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *ESOP8 dimensions(mm)*.

Table 3. ESOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30		1.70
b	0.33		0.51
c	0.19		0.25
D	4.80	4.90	5.00
D1	3.15		3.45
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.26		2.56
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1601WGTR-I	ESOP8	Green	Tape & Reel	4000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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