4.5V~100V, 2A, Synchronous Step-down Converter

1 Features

- 4.5V to 100V Wide Operational Range
- Output Current Capability: 2A
- Integrated High Side Power MOS with 400mΩ Low Resistance
- Integrated Low Side Power MOS with 120mΩ Low Resistance
- Constant-On-Time Control
- Low Quiescent: 240μA
- Low Input Current at Off-state: 4μA
- Programmable Switching Frequency from 300kHz to 800kHz
- FPWM/PFM mode selectable
- Built-in Pull-up Current at EN Pin
- Internal 2ms Soft Start
- Integrated BST Charge Circuit
- Low Drop Out Mode Support 97% Duty Cycle
- Pre-bias Start-up
- Available in ESOP8 package

2 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry application

3 Description

The GD30DC1902 is a 100V, 2A synchronous step-down converter featuring integrated high-side and low-side MOSFETs. Utilizing advanced constant-on-time (COT) control, it offers a compact solution size with excellent load transient performance.

The integrated BST charging circuit reduces both cost and solution size. Its extended high-duty cycle makes it ideal for applications requiring a low drop-out feature. 240μA quiescent current saves the power, while its low off-current is particularly suitable for battery-powered applications.

The GD30DC1902 supports FCCM/PFM mode selection. FCCM mode ensures continuous conduction operation across all load ranges, enabling compatibility with isolated buck converter applications.

It includes built-in protection features such as cycle-by-cycle current limit, hiccup mode SCP, output over-voltage protection (OVP), feedback (FB) open protection, and thermal shutdown for excessive power dissipation.

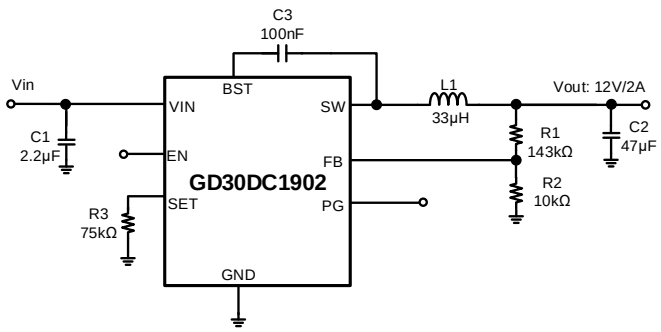
The GD30DC1902 is available in a compact ESOP8 package, making it a space-efficient solution.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1902	ESOP8	4.9mm x 3.9mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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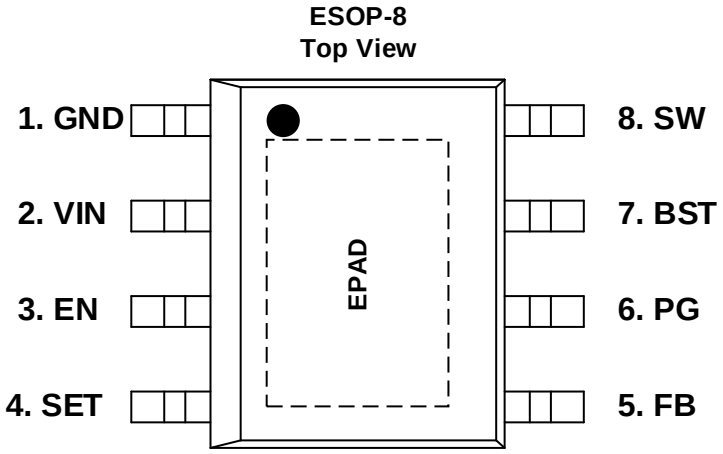
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	ESOP8		
GND	1	G	**Ground Pin.** Chip's GND connection. Connect to the ground of the system.
VIN	2	P	**Power supply**. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
EN	3	I	**Enable**. Pull high to enable the output. and pull low to disables the device and turns it into shutdown. Don't leave this pin floating.
SET	4	I	**Set Pin**. Frequency and Mode selection.
FB	5	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider from VOUT to GND.
PG	6	O	**Power Good Indicator**. Open drain structure. Need connect to an external voltage source through a pull-up resistor(e.g. 100kΩ). Floating it if not used.
BST	7	O	**Bootstrap**. Connect a high-quality BST capacitor between SW and BST to form a floating supply across the high-side switch driver.
SW	8	O	**Switch output**. Switching node of power stage. Connected to the internal MOSFET switches and inductor terminal.
EPAD	9	G	**Exposed Pad.** Connect the exposed pad to the PCB GND plane to ensure optimal thermal efficiency.

1. I = Input, O = Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Power supply	−0.3	105	V
V_{SW}	Switching node of power stage	−0.3	105	V
V_{BST}-V_{SW}	Bootstrap pin for high side power MOS driving.		6	V
I_{EN}	Max Input current into EN pin		100	μA
All Other Pins		−0.3	6	μA
T_J	Junction temperature	−40	150	°C
T_{STG}	Storage temperature	−65	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Power supply pin	4.5		100	V
V_{OUT}	Output voltage	0.8		28	V
I_{OUT}	Continues Output current	0		2	A
T_J	Junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Junction to ambient thermal resistance	ESOP8	48	°C/W
$\Theta_{JC(TOP)}$	Junction to case (top) thermal resistance	ESOP8	52	°C/W
$\Theta_{JC(BOT)}$	Junction to case (bottom) thermal resistance	ESOP8	2.3	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 60V and T_J = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input UVLO and Quiescent Current						
VIN_{UVR}	VIN UVLO rising threshold			4.3		V
VIN_{UVF}	VIN UVLO falling threshold			4		V
VIN_{UV_hys}	VIN UVLO hysteresis			0.3		V
I_S	Shutdown supply current	EN=0V		4		μA
I_Q	Quiescent supply current	FB=0.82V		240		μA
EN SECTION						
V_{EN_R}	Enable rising threshold			1.2		V
V_{EN_F}	Enable falling threshold			1		V
$I_{EN\_PULL\_UP}$	Enable pull up current	V_{EN}=L		1		μA
		V_{EN}=H		4.5		
V_{EN_CLAMP}	EN clamp voltage	EN voltage at 100μA current		6		V
FEEDBACK SECTION						
V_{FB}	Feedback voltage		0.768	0.78	0.792	V
V_{FB_UV}	Feedback voltage under voltage threshold			90		mV
POWERSTAGE SECTION						
R_{HSON}	High Side MOS ON resistance	BST-SW=5V		400		mΩ
R_{LSON}	Low side MOS ON resistance			120		mΩ
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
Current limit SECTION						
I_{LIMIT_HS}	HS current limit threshold			3		A
SOFT START SECTION						
T_{SS}	Soft-start time	V_{FB} from 10% to 90%		2		ms
Frequency SECTION						
F_{SW}	FPWM Mode Switching Frequency	SET Pin short to GND		300		KHz
		R_{SET} = 18.7K		500		
		R_{SET} = 37.4K		800		
	PFM Mode Switching Frequency	R_{SET} = 75K		300		
		R_{SET} = 150K		500		
		SET Pin Float		800		
T_{ON_MIN}	Min On pulse[1]			120		ns
T_{ON_MAX}	Max On pulse			10		μs
T_{OFF_MIN}	Min Off time[1]			350		ns
Power Good						

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{PG_UV}	FB falling			87		%
	FB rising			93		%
V_{PG_OV}	FB falling			106		%
	FB rising			112		%
R_{PG_ON}		Sink 3mA		55		Ω
T_{PG_DELAY}	PG falling delay time			12		μs
OVER TEMP SECTION						
T_{OTP_R}	Over temperature protection rising threshold[1]			140		°C
T_{OTP_F}	Over temperature protection falling threshold[1]			120		°C

1. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

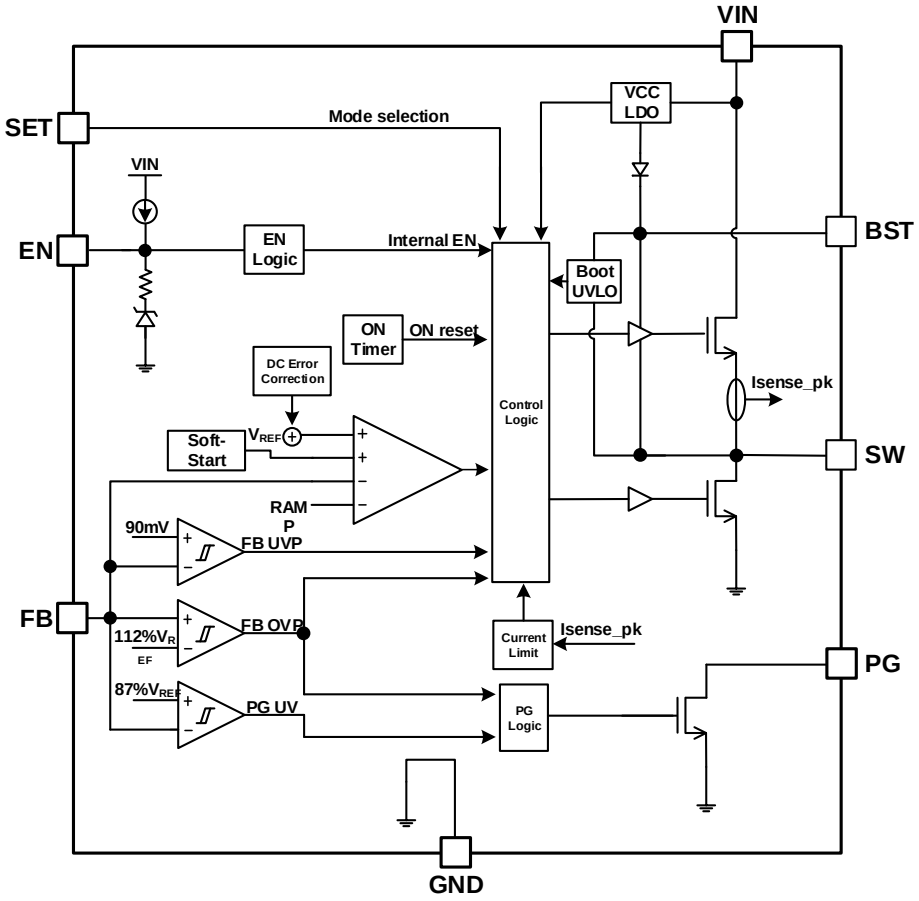


Figure 1 GD30DC1902 Functional Block Diagram

6.2 Operation

6.2.1 COT control loop operation

The GD30DC1902 is a fully integrated synchronous step-down switch-mode converter. It utilizes constant-on-time (COT) control to achieve fast transient response and simplify loop stabilization. At the start of each cycle, the high-side MOSFET (HS-FET) is activated when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), signaling that the output voltage is insufficient. The on-time duration is determined by both the input and output voltages, ensuring relatively stable switching frequency across the input voltage range.After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when VFB drops below VREF. Through this repetitive process, the converter regulates the output voltage.

The integrated low-side MOSFET (LS-FET) activates when the HS-FET is off, minimizing conduction losses. If both the HS-FET and LS-FET are simultaneously on, it creates a short circuit between the V_{IN} and GND, referred to as shoot-through. To prevent this, an internal dead time (DT) is employed between the transitions of HS-FET turning off and LS-FET turning on, or LS-FET turning off and HS-FET turning on.

In FPWM (Forced Pulse Width Modulation) mode, the LS-FET remains on continuously until the next HS-FET pulse arrives. Conversely, in PFM (Pulse Frequency Modulation) mode, the LS-FET switches off when the inductor current drops to zero, causing the IC to enter a hi-z state until the next HS-FET pulse arrives. For detailed operational instructions, refer to the section below.

6.2.2 Light Load operation

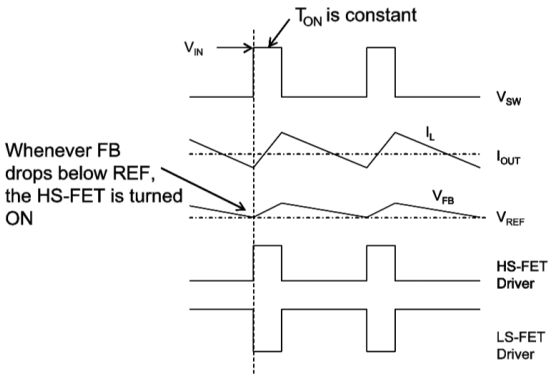


Figure 2 FPWM Operation

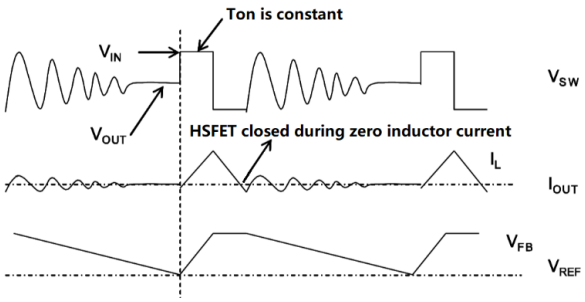


Figure 3 PFM Operation

The GD30DC1902 can be configured to work in either FPWM mode or PFM mode, as is shown in above Figure 2 and Figure 3.

In FPWM mode, the switching frequency remains stable as the load current varies. This helps reduce output voltage (V_{OUT}) ripple under light loads and simplifies the design of second-stage filters for damping power stage noise. However, because the internal power MOSFETs switch on and off more frequently, light-load efficiency is lower compared to PFM mode.

In PFM mode under light-load conditions, the V_{FB} cannot reach the V_{REF} while the inductor current approaches zero. The current modulator then takes over, keeping the inductor current near zero. During this time, the LS-FET driver enters a high-impedance (Hi-z) state, resulting in a slow output voltage drop. Consequently, the GD30DC1902 naturally reduces its switching frequency, achieving higher efficiency. However, as a trade-off, PFM mode experiences greater output voltage ripple.

For detailed setup methods regarding the operating mode and switching frequency of the GD30DC1902, refer to the section *Operation mode and frequency selection*.

6.2.3 Heavy Load operation

For FPWM mode, the operating mechanism is the same as that in light load condition.

For PFM mode, As the output current rises from a light-load state, the regulation period of the current modulator becomes shorter. The HS-FET is activated more frequently, leading to an increase in the switching frequency. When the modulation time reduces to zero, the output current reaches the critical level. The critical output current can be calculated using the Equation(1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

6.2.4 Enable (EN) Control

The GD30DC1902 includes a dedicated enable control pin with positive logic. To activate the regulator, apply a voltage above 1.2V (typical) to the EN pin, and to disable it, set the EN pin voltage below 1V (typical). By using two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin. It recommend to use less than 30KΩ resistor for R_{ENDN}.

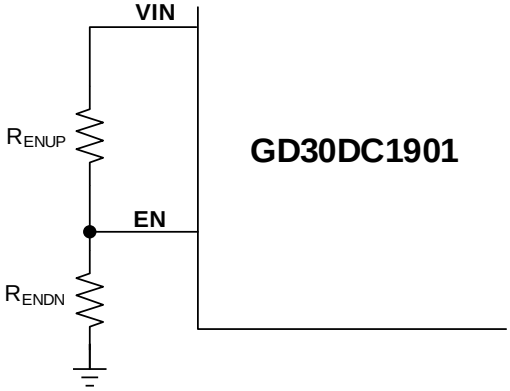


Figure 4 EN divider for adjustable UVLO

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 1 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} - 4uA \times R_{ENUP} \quad (3)$$

6.2.5 Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) feature ensures the chip does not operate at inadequate supply voltages. The GD30DC1902 UVLO comparator monitors the input voltage, with a rising threshold of approximately 4.3V and a falling threshold of 4V.

6.2.6 Internal Soft Start (SS)

The soft-start (SS) function prevents output voltage overshoot during start-up. When the chip powers on, the internal circuit generates a soft-start voltage (V_{SS}) that gradually increases from 0V to 1V. While V_{SS} remains below V_{REF}, V_{SS} replaces V_{REF} as the reference for the error amplifier. Once V_{SS} surpasses V_{REF}, the error amplifier switches back to using V_{REF}. The soft-start duration is internally set to 2ms.

6.2.7 Operation mode and frequency selection

The GD30DC1902 provides both FPWM and PFM in light-load condition. The FM PIN can determine the switching frequency too. GD30DC1902 has four options for switching frequency and operation mode selection via choosing different value resistors between FM and GND. Refer below for detail.

Table 1 Switching frequency set resistor selection

SET	Operation Mode	Switching Frequency
SET Pin short to GND	FPWM	300kHz
RSET = 18.7kΩ	FPWM	500kHz
RSET = 37.4kΩ	FPWM	800kHz
RSET = 75kΩ	PFM	300kHz
RSET = 150kΩ	PFM	500kHz
SET Pin Float	PFM	800kHz

6.2.8 Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The GD30DC1902 incorporates both peak current limit and valley current limit controls. During HS-FET operation, its current is monitored, and the HS-FET turns off upon reaching the peak current limit, enabling the LS-FET valley current limit control. The LS-FET remains active until its current falls below the valley limit. Once OCP occurs, the output voltage will drop down at the same time, which will cause VFB dropping down correspondingly, either 'VFB below FB UVP threshold(typically 140mV)' or 'OCP is occurred' happen, the device will start to timing typically 10ms deglitch time, if any of the above two conditions still exists, the device will enters GD30DC1902 will enter hiccup mode, until both of the conditions are removed, then the GD30DC1902 will back to normally switching again.

6.2.9 Power Good Indication

The GD30DC1902 uses a power-good (PG) output to indicate whether the output voltage of the buck regulator ready or not. The PG pin is an open drain output. Once the FB pin is between 87% and 112% of the internal voltage reference the PG pin is de-asserted and the pin floats. A pull-up resistor of 10 kΩ to 100kΩ to a voltage source that is 5.5 V or less is recommended. A higher pull-up resistance reduces the amount of current drawn from the pull-up voltage source when the PG pin is asserted low. A lower pull-up resistance reduces the switching noise seen on the PG signal. The PG is in a defined state once the input voltage is greater than 2 V but with reduced current sinking capability. The PG will achieve full current sinking capability as input voltage approaches 3 V. The PG pin is pulled low when the FB is lower than 87% or greater than 112% of the nominal internal reference voltage. Also, PG is pulled low, if UVLO or thermal shutdown are asserted or the EN pin pulled low.

6.2.10 Thermal Shutdown

The GD30DC1901 includes thermal shutdown protection, with its junction temperature monitored internally. If the temperature exceeds the threshold (typically 140°C), the converter shuts down. This protection is non-latching, allowing the GD30DC1901 to automatically restart once the temperature decreases.

7 Application Information

7.1 Typical Application Circuit

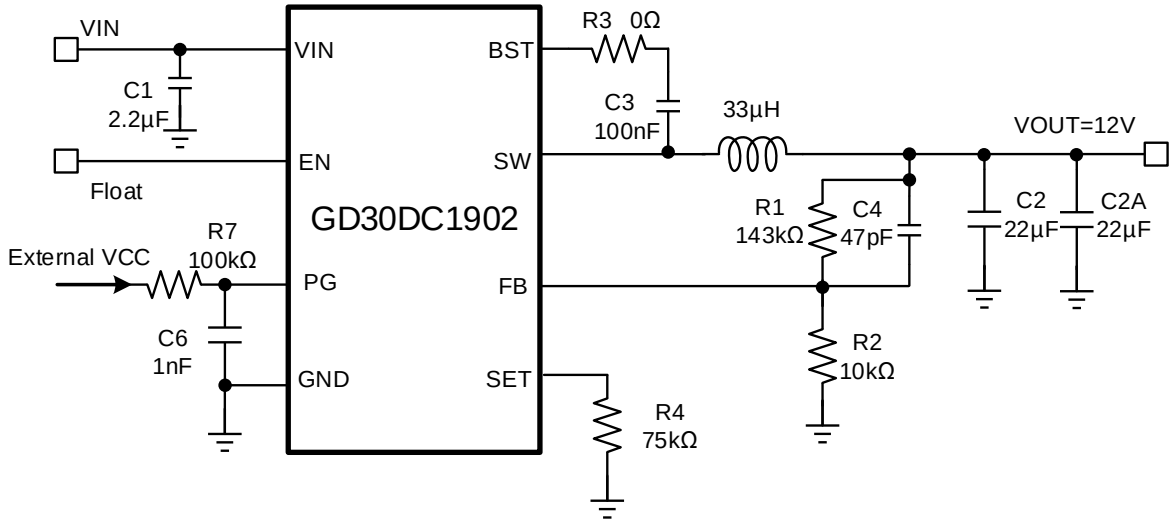


Figure 5 VIN=48V, VOUT=12V, IOUT=2A, FSW=300KHz, PFM MODE

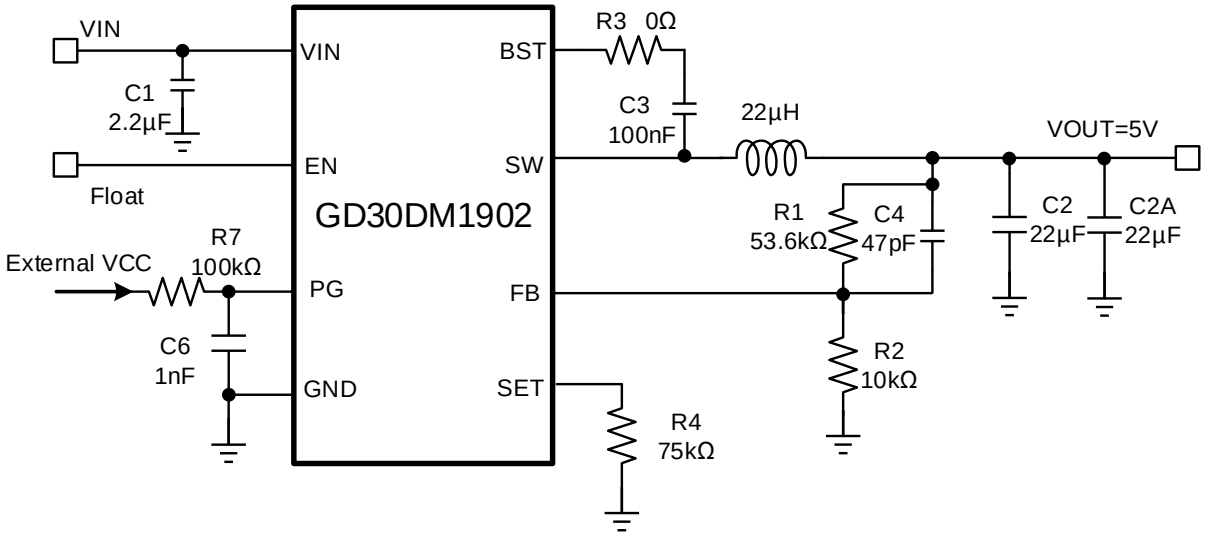


Figure 6 VIN=48V, VOUT=5V, IOUT=2A, FSW=300KHz, PFM MODE

7.2 Detailed Design Description

7.2.1 Setting the Output Voltage

The GD30DC1902 output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.78V. The feedback network is shown in Figure 7.

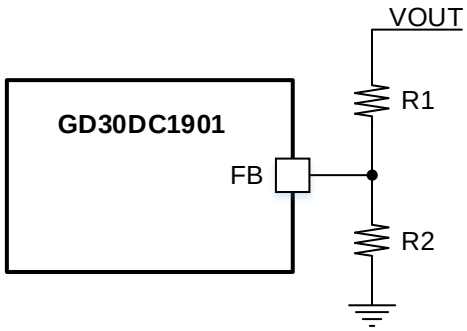


Figure 7 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT2} = \frac{(V_{OUT1} + V_F) \times N_S}{N_P} \quad (4)$$

7.2.2 Selecting the Inductor

An inductor is essential for providing continuous current to the load while being driven by the switched input voltage. A larger inductor minimizes ripple current and reduces output voltage ripple but comes with drawbacks such as a larger physical size, higher series resistance, and lower saturation current. For most designs, the suitable inductance value can be calculated using the following Equation(5):

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (5)$$

Where ΔIL is the inductor ripple current.

Table 2 lists the recommended feedback resistor values for common output voltages (F_{SW}=300kHz).

Table 2 Resistor Selection for Common Output Voltages[1]

VOUT(V)	R1(kΩ)	R2(kΩ)	Cff(pF)	L(μH)	COUT(μF)
12	143	10	47	33	2*22
5	53.6	10	47	22	2*22

1. For a detailed design circuit, please refer to the Typical Application Circuits.

7.2.3 Selecting the Output Capacitor

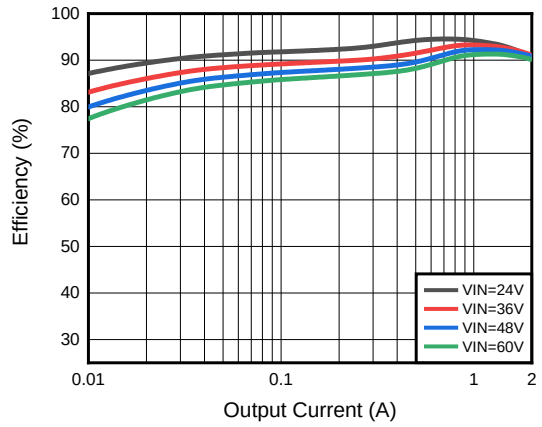
The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation(6):

$$\Delta V_{OUT1} = \frac{I_{OUT2} \times V_{OUT1} \times N_S}{f_{SW} \times C_{OUT1} \times V_{IN} \times N_P} \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. The characteristics of the output capacitor also affect the stability of the regulation system. The GD30DC1902 can be optimized for a wide range of capacitance and ESR values.

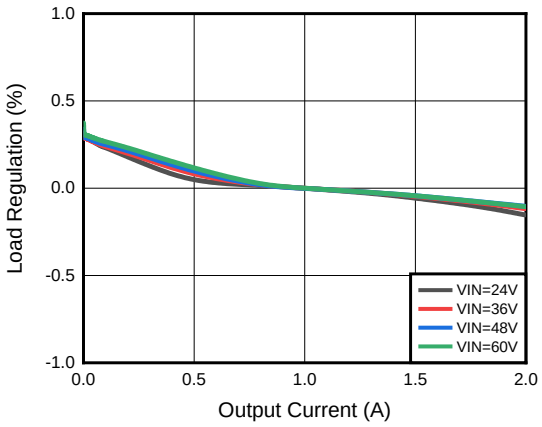
7.3 Typical Application Curves

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 33μH, F_{SW}=300kHz, and T_A = +25°C, unless otherwise noted.



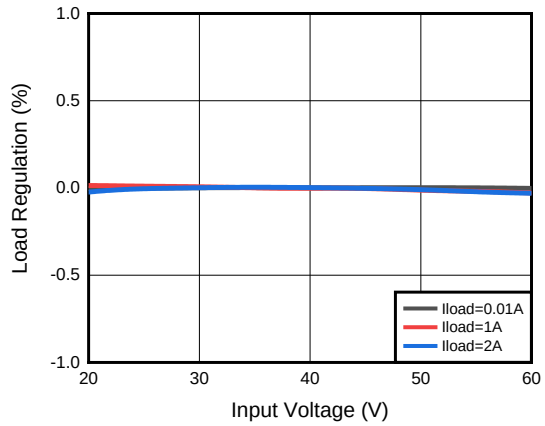
PFM MODE, DCR=65mΩ

Figure 8 Efficiency vs. Load Current



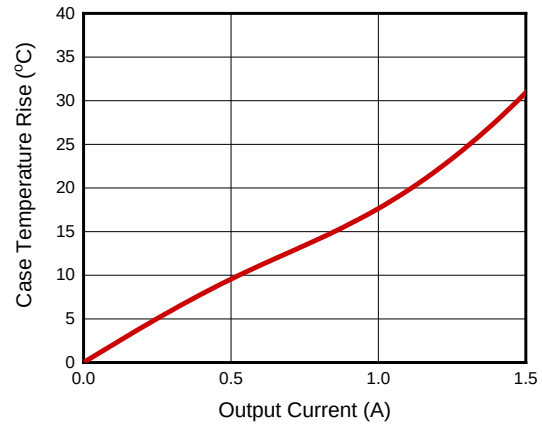
PFM MODE, DCR=65mΩ

Figure 9 Load Regulation



PFM MODE, DCR=65mΩ

Figure 10 Line Regulation

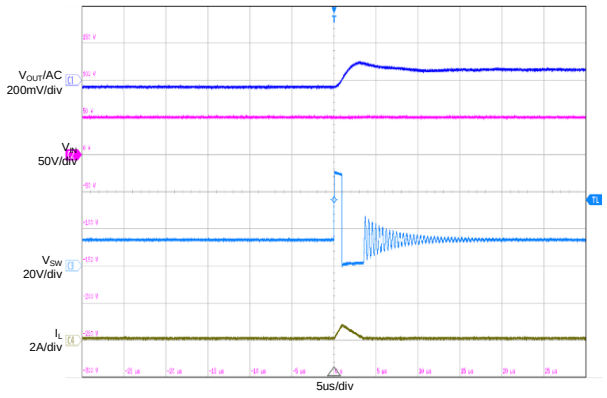


PFM MODE, no air flow

Figure 11 Thermal Rise

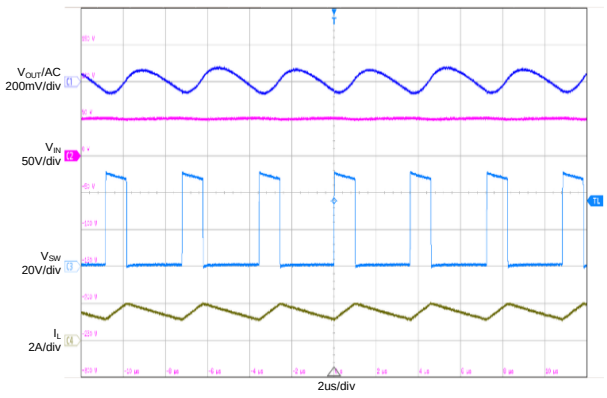
Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 33μH, F_{SW}=300kHz, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



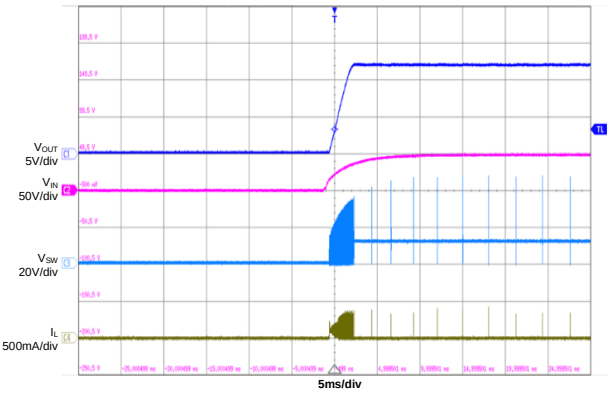
I_{OUT}=0A, PFM MODE

Figure 12 Output Voltage Ripple



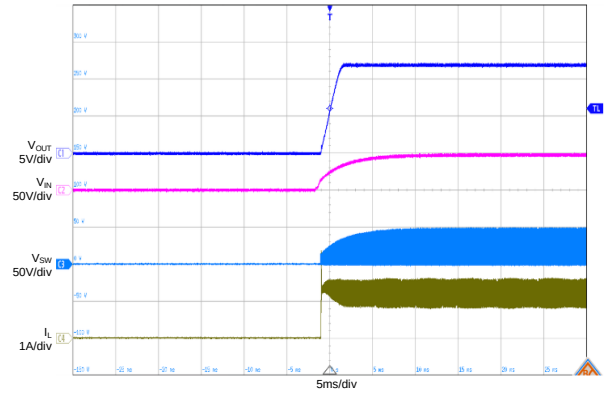
I_{OUT}=2A

Figure 13 Output Voltage Ripple



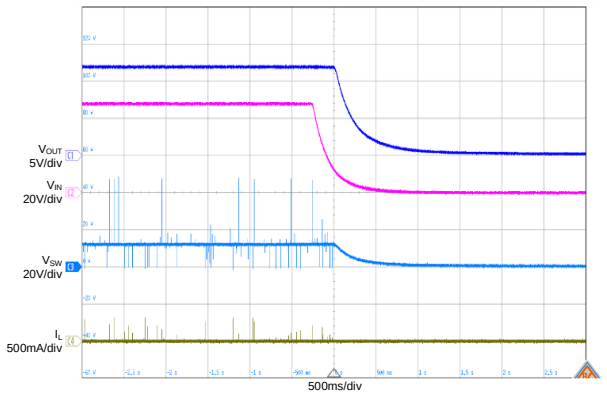
I_{OUT}=0A, PFM MODE

Figure 14 Start-Up through VIN



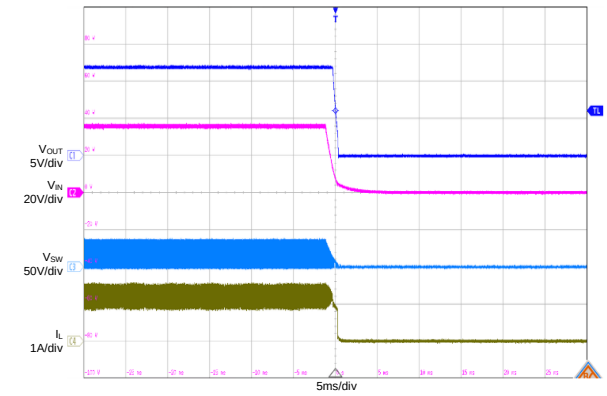
I_{OUT}=2A

Figure 15 Start-Up through VIN



I_{OUT}=0A, PFM MODE

Figure 16 Shut-Down through VIN

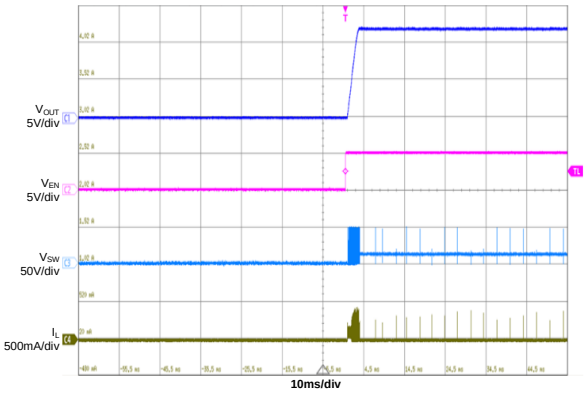


I_{OUT}=2A

Figure 17 Shut-Down through VIN

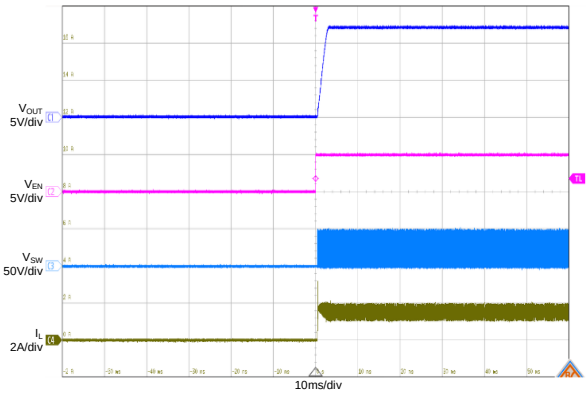
Typical Application Curves (continued)

V_{IN} = 48V, V_{OUT} = 12V, C_{IN} = 2.2μF, C_{OUT} = 2x22μF, L1 = 33μH, F_{SW}=300kHz, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



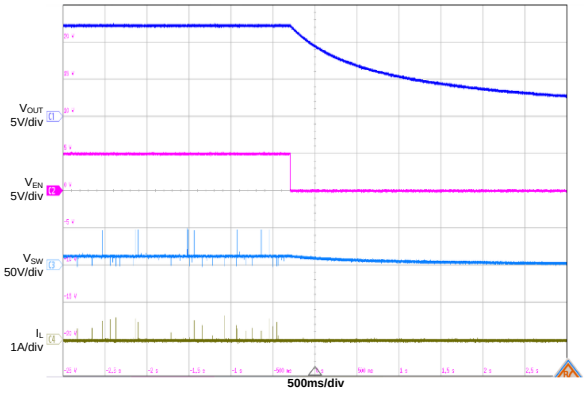
I_{OUT}=0A, PFM MODE

Figure 18 Start-Up through EN



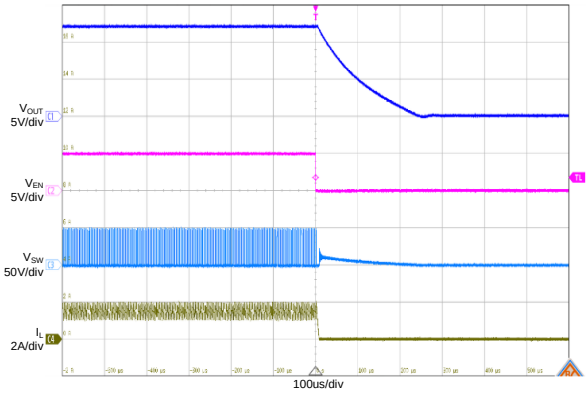
I_{OUT}=2A

Figure 19 Start-Up through EN



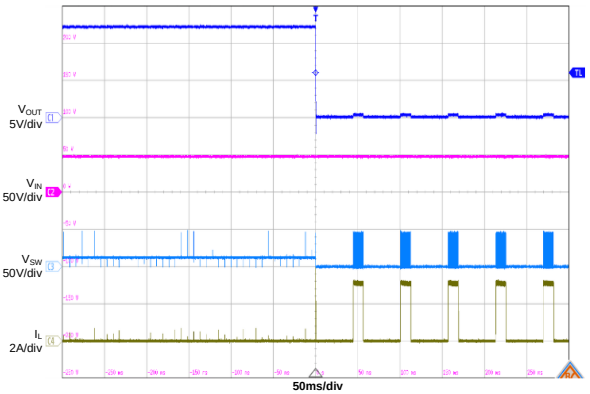
I_{OUT}=0A, PFM MODE

Figure 20 Shut-Down through EN



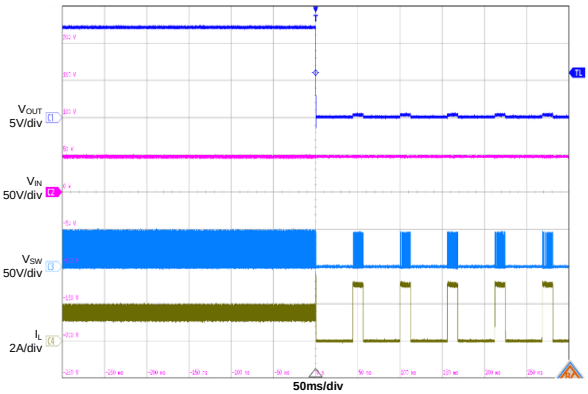
I_{OUT}=2A

Figure 21 Shut-Down through EN



I_{OUT}=0A, PFM MODE

Figure 22 Short-Circuit Entry

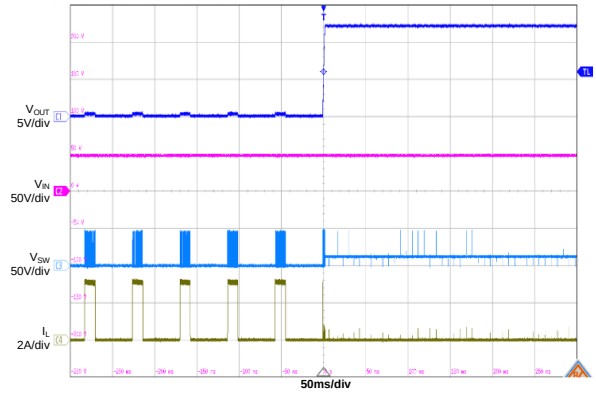


I_{OUT}=2A

Figure 23 Short-Circuit Entry

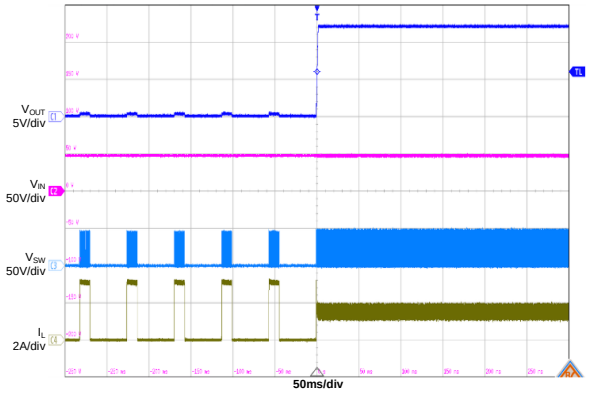
Typical Application Curves (continued)

V_{IN} = 3.3V, V_{OUT} = 1V, C_{IN} = 2*22μF, C_{OUT} = 4*22μF, and T_A = +25°C, unless otherwise noted.



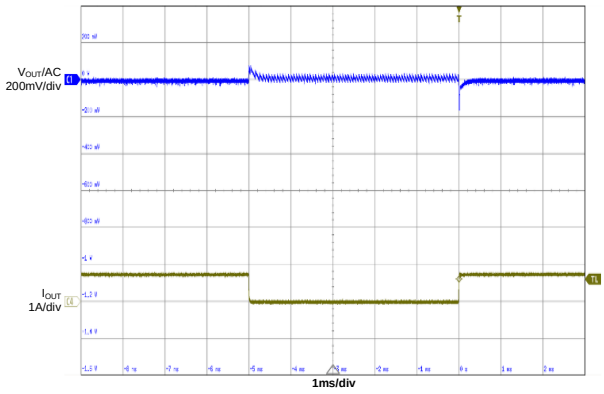
I_{OUT}=0A, PFM MODE

Figure 24 Short-Circuit Recovery



I_{OUT}=2A

Figure 25 Short-Circuit Recovery



I_{OUT} = 1A to 2A, slew rate=3A/μs setting by E-load

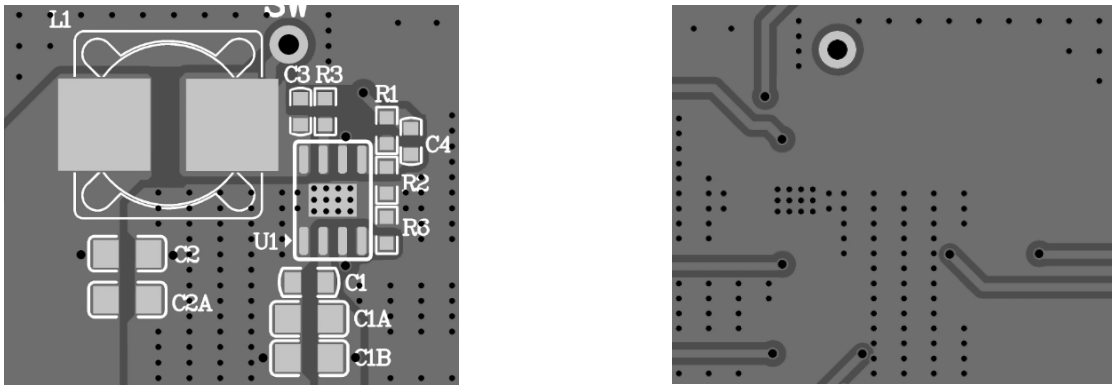
Figure 26 Load Transient

8 Layout Guidelines and Example

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

1) Place the input capacitor as close to VIN and GND as possible.
2) Place the external feedback resistors as close to FB as possible.
3) Keep the switching node (such as SW, BST) far away from the feedback network. Ensure BST and SW trace as short as possible.
4) Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

For best results, follow the layout example below.



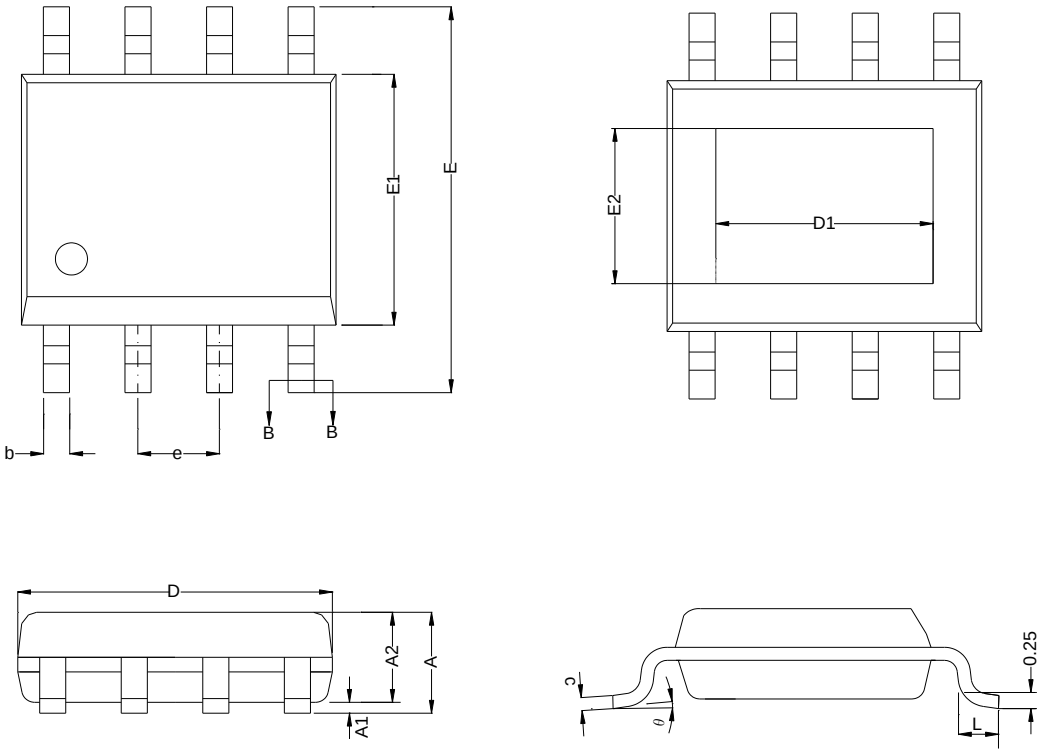
Top Layer **Bottom Layer**

Figure 27 Typical GD30DM1106 Example Layout

9 Package Information

9.1 Outline Dimensions

ESOP8 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *ESOP8 dimensions(mm)*.

Table 3. ESOP8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30		1.70
b	0.33		0.51
c	0.19		0.25
D	4.80	4.90	5.00
D1	3.15		3.45
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.26		2.56
e		1.27	
e1		0.10	
L	0.50	0.60	0.80
θ	0°		8°

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1902WGTR-I	ESOP8	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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