ZX3803
DATASHEET
V1.0

AXTEK Technology Company Limited

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Chip Overview

The ZX3803 is a highly integrated contactless communication chip operating at 13.56 MHz, supporting reader/writer modes compliant with ISO/IEC 14443 Type A and Type B protocols. It also provides a low-power card detection function, making it suitable for battery-powered reader devices that require low power consumption while being able to process external cards entering the RF field in real time. The product features low voltage operation, low power consumption, strong driving capability, multi-interface support, and multi-protocol compatibility. It is ideal for contactless reader applications with requirements for low power, low voltage, and low cost.

Typical Applications

The ZX3803 supports various microcontroller interface types that can be directly connected, such as SPI, I2C, and UART. The microcontroller interface is identified through the logic level on the control pin after the reset phase. Designed for applications in the financial secto, contactless door locks, access control, and various card reader devices, this low-voltage, low-cost chip complies with ISO/IEC 14443 Type A/Type B protocols and operates at a high frequency of 13.56 MHz. It features high integration and ultra-low power consumption. The typical application block diagram is shown below.

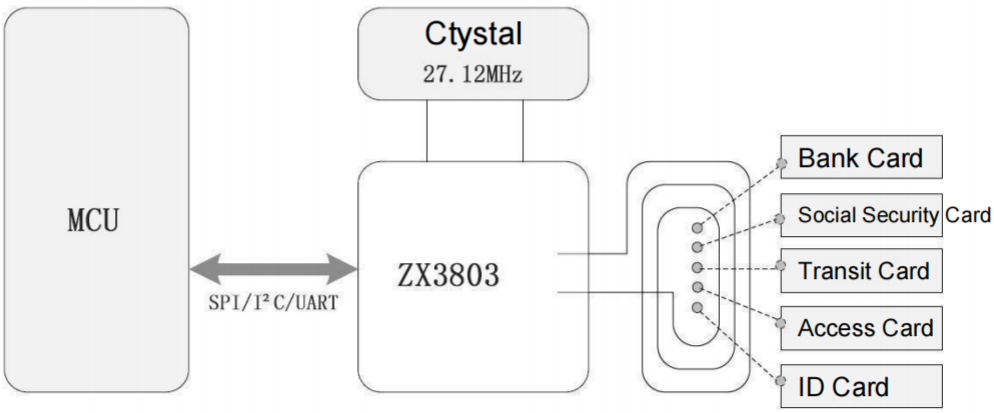


Figure 1. Typical Application Block Diagram

Product Features

- Compliant with ISO/IEC 14443 Type A/B standards
- Supports Low Power Card Detection (LPCD) function
- Multiple host interfaces supported:
  - >> SPI interface up to 10 Mbit/s
  - >> I2C interface supporting Fast Mode up to 400 kbit/s
  - >> Serial UART interface with maximum communication rate of 1,228.8 kbit/s
- Built-in power amplifier with adjustable transmit power
- Adjustable receive gain
- External clock: 27.12 MHz
- Supports data rates of 106 kbit/s, 212 kbit/s, and 424 kbit/s
- 64-byte transmit/receive FIFO buffer
- Built-in CRC controller
- Programmable timers
- Flexible and configurable interrupt output modes
- Operating voltage: 2.0 V – 5.5 V
- Separate analog, digital, and transmit power supplies
- Power-saving modes including hardware and software power-down
- Supports TIN and TOUT
- Crystal fast-startup function supported
- EMV under/overshoot optimization feature
- Built-in temperature sensor with automatic RF transmission shutdown at high temperature
- Programmable I/O pins
- Packaging options: QFN32, SOP16

Pin Definitions

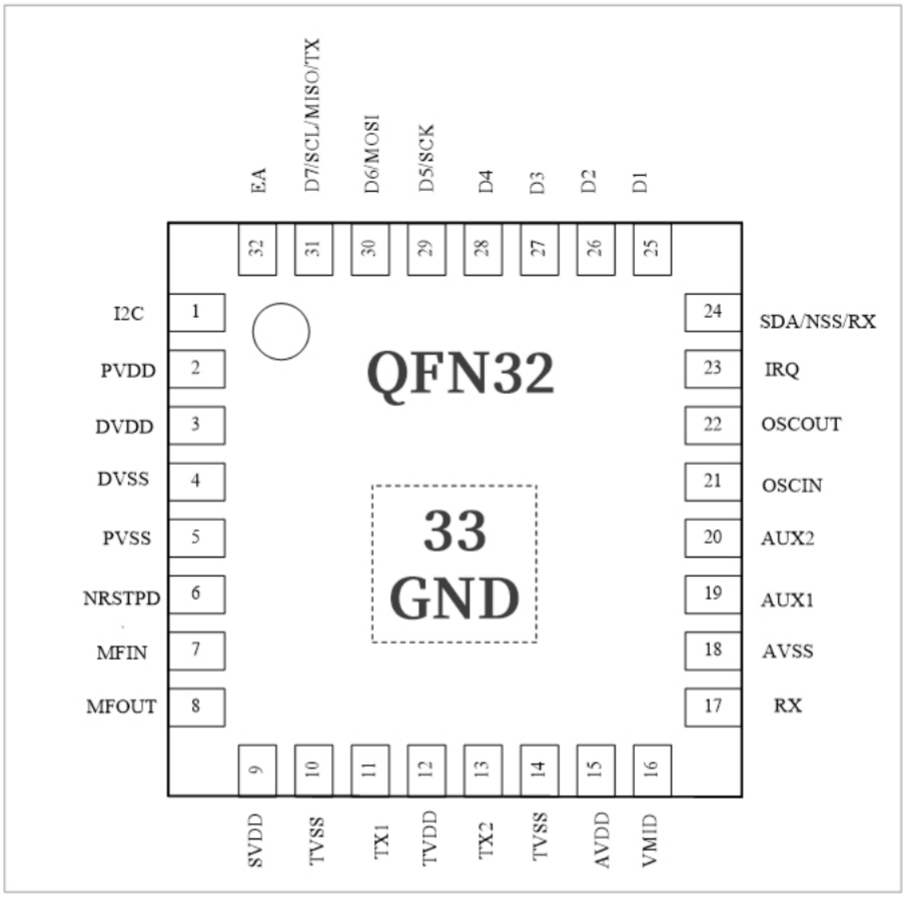


Figure 2. QFN32 Package Pin Layout

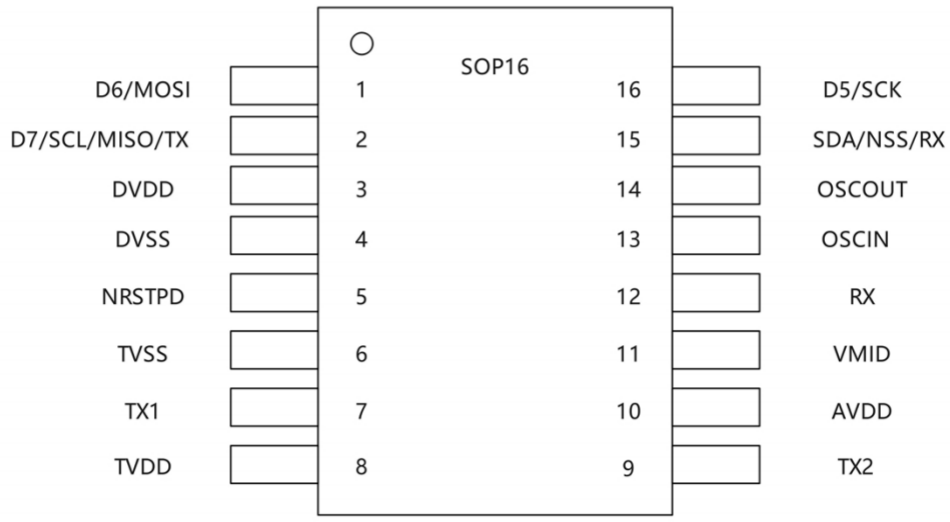


Figure 3. SOP16 Package Pin Layout

The pin functions are described in the table below:

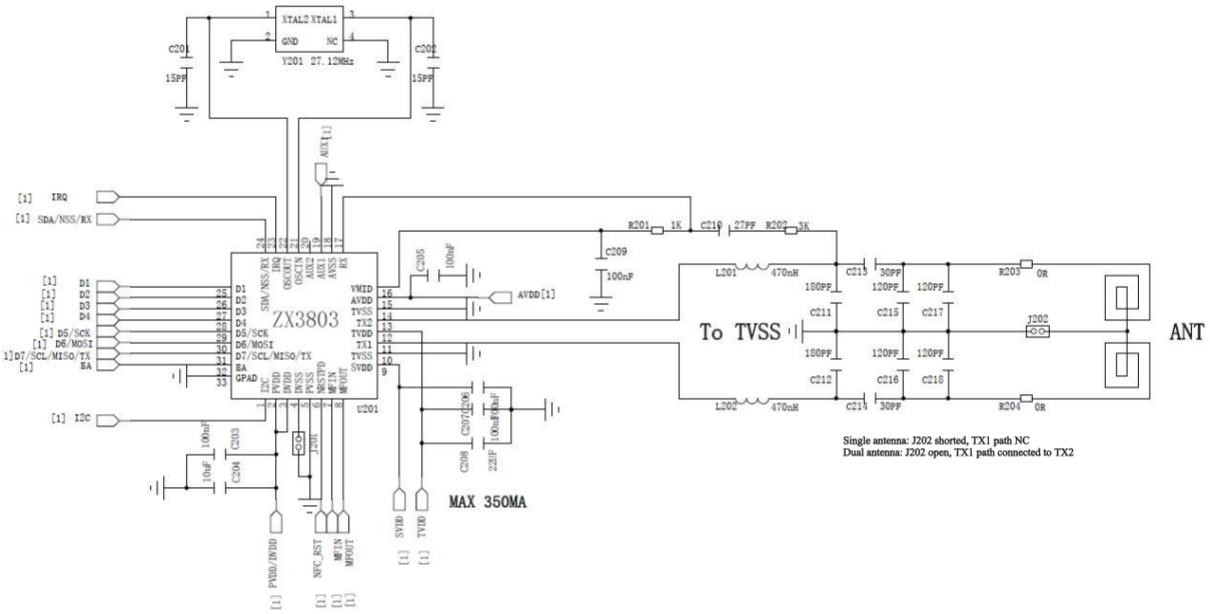
QFN32 NO.	SOP16 NO.	Name	I/O	Function Description
1		I2C	I	I2C interface enable, active high
2		PVDD	P	Pin power supply
3	3	DVDD	P	Digital power supply
4	4	DVSS	P	Digital ground
5		PVSS	P	Pin ground
6	5	NRSTPD	I	Reset/Power-down pin, active low
7		MFIN	I	Signal input
8		MFOUT	O	Signal output
9		SVDD	P	MFIN/MFOUT power supply
10	6	TVSS	P	Transmit circuit ground
11	7	TX1	O	Transmit output pin 1, outputs modulated 13.56 MHz carrier signal
12	8	TVDD	P	Transmit circuit power supply
13	9	TX2	O	Transmit output pin 2, outputs modulated 13.56 MHz carrier signal
14		TVSS	P	Transmit circuit ground
15	10	AVDD	P	Analog circuit power supply
16	11	VMID	P	Internal reference voltage
17	12	RX	I	RF input pin
18		AVSS	P	Analog ground
19		AUX1	O	Test output 1
20		AUX2	O	NC
21	13	OSCIN	I	Clock input 27.12 MHz
21	14	OSCOUT	O	Clock output 27.12 MHz
22		IRQ	O	Interrupt output pin
24	15	SDA/NSS/RX	I	Digital communication interface, depending on the selected communication mode I2C: SDA / SPI: Slave Select / UART: RX
25		D1	I/O	Parallel communication interface / I2C slave address selection bit ADDR5
26		D2	I/O	Parallel communication interface / I2C slave address selection bit ADDR4
27		D3	I/O	Parallel communication interface / I2C slave address selection bit ADDR3
28		D4	I/O	Parallel communication interface / I2C slave address selection bit ADDR2

[1] I 输入引脚； O 输出引脚； P 电源引脚。

29	16	D5/SCK	I/O	Parallel communication interface / I2C slave address selection bit ADDR1 / SPI interface clock input, depending on the selected communication mode
30	1	D6/MOSI	I/O	Parallel communication interface / I2C slave address selection bit ADDR0
31	2	D7/SCL/MISO/TX	I/O	Parallel communication interface / I2C slave SCL / SPI slave output / UART TX, depending on the selected communication mode
32		EA	I	I2C address encoding enable
33		VSS	P	Ground

Application Circuit Diagram

The recommended application circuit for the ZX3803 uses the SPI communication interface. It employs a dual-antenna configuration, with the center tap of the coil connected to ground. Pin 33 refers to the large pad on the bottom of the chip, which must be properly grounded. The values of C8, C9, C11, and C13 in the diagram should be adjusted according to actual conditions.



Note: RF matching should be finalized based on actual physical testing and tuning results.

Communication Mode Selection

The ZX3803 supports three communication modes: SPI, I2C, and UART.

Communication Interface Selection				
Pin No.	**PIN Name**	**UART**	**SPI**	**I2C**
1	I2C	0	0	1
32	EA	0	1	EA
31	D7	TX	MISO	SCL
30	D6	MX	MOSI	ADDR_0
29	D5	DTRQ	SCK	ADDR_1
28	D4	-	-	ADDR_2
27	D3	-	-	ADDR_3
26	D2	-	-	ADDR_4
25	D1	-	-	ADDR_5
24	SDA	RX	NSS	SDA

Note: " -" indicates " don' t care."

Electrical Specifications

Operating Range

Symbol	Parameter	Condition	Min	Typical	Max	Unit
DVDD	Digital Supply Voltage	PVSS=DVSS=AVSS=TVSS=0V PVDD=DVDD<=AVDD<=TVDD	2.0	3.3	5.5	V
AVDD	Analog Supply Voltage					
TVDD	Transmitter Supply Voltage					
PVDD	Pin Supply Voltage	PVSS=DVSS=AVSS=TVSS=0V PVDD=DVDD<=AVDD<=TVDD	2.0	3.3	5.5	V
T_{OPR}	Operating Temperature	-	-40	25	85	℃
ESD	Maximum Discharge Voltage	ESDA/JEDEC JS-001-2023; (Zap 1 pulse,Interval: >=0.1S)	-	-	2	KV

DC Parameters

The values listed in the table are measured under normal operating conditions at 25°C.

Symbol	Parameter	Condition	Min	Max	Unit
V_{IL}	Input Low Voltage	DVDD = 2.7~5V	0	0.3*DVDD	V
V_{IH}	Input High Voltage	DVDD=2.7~5V	0.7*DVDD	1.1*DVDD	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA , DVDD=5V	0	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -1.8mA , DVDD=5V	DVDD-1.0	DVDD	V
I_{LI}	Input Leakage Current	V_{IN} = -0.5~5.5V	0	100	nA
C_{IO}	I/O Pin Parasitic Capacitance	f = 1.0MHz, T_{OPR} = 25°C	-	5	pF
VMID	Reference Voltage	AVDD = 2.7~5.5V	0.5*AVDD-0.15V	0.5*AVDD+0.15V	V

3.3V Electrical Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Unit
I_{HPD}	Hardware Power-Down Current	AVDD=DVDD=PVDD=TVDD=3.3V NRSTPD=LOW	-		-	μA
I_{SPD}	Software Power-Down Current	AVDD=DVDD=PVDD=TVDD=3.3V	-	0.6	-	μA
I_{DVDD}	Digital Supply Current	Normal Operating Condition，DVDD=3.3V	-	2	-	mA
I_{AVDD}	Analog Supply Current	Normal Operating Condition，AVDD=3.3V	-	2	-	mA
I_{TVDD}	Transmitter Circuit Current	Normal Operating Condition，TVDD=3.3V	-	-	100	mA

5.0V Electrical Specifications

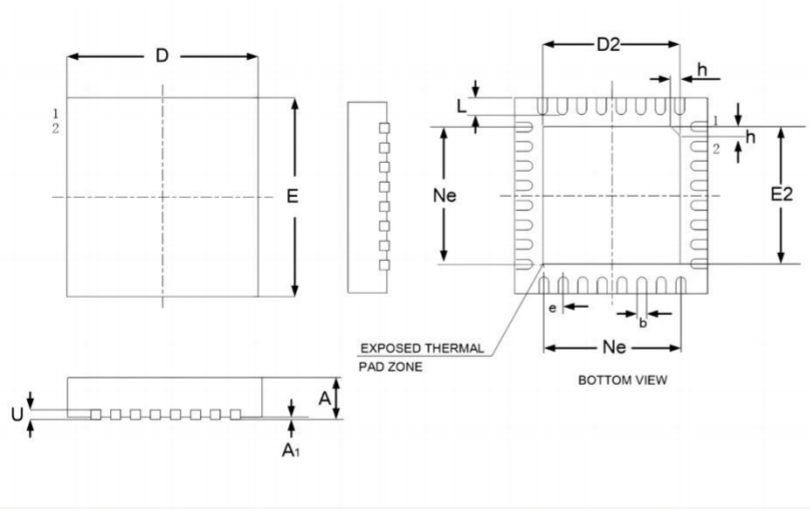
Symbol	Parameter	Condition	Min	Typical	Max	Unit
I_{HPD}	Hardware Power-Down Current	AVDD=DVDD=PVDD=TVDD=5V NRSTPD=LOW	-		-	μA

I_{SPD}	Software Power-Down Current	AVDD=DVDD=PVDD=TVDD=5V	-	0.6	-	μA
I_{DVDD}	Digital Supply Current	Normal Operating Condition，DVDD=5V	-	2	-	mA
I_{AVDD}	Analog Supply Current	Normal Operating Condition，AVDD=5V	-	2	-	mA
I_{TVDD}	Transmitter Circuit Current	Normal Operating Condition，TVDD=5V	-	60	-	mA

AC Parameters

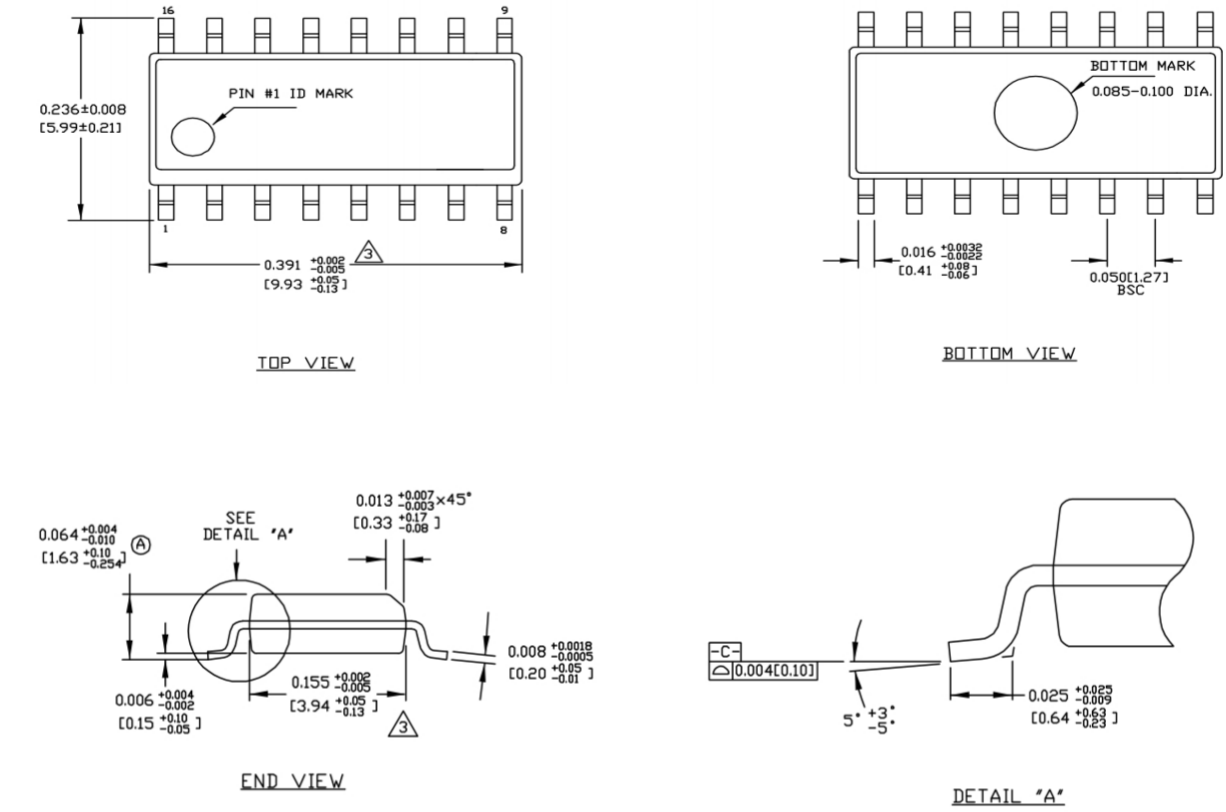
Symbol	Parameter	Min	Typical	Max	Unit
fosc	Oscillation Frequency	-	27.12	-	MHz
Tosc	Crystal Normal Startup Time		500		μS
Tfosc	Crystal Fast Startup Time		150		μS
t1	RF Turn-Off Time	-	5		μS
t2	RF Turn-On Time	-	5		μS
t3	Receiver Circuit Setup Time (AVDD = 5V)	-	1.2		mS
t4	Receiver Circuit Setup Time (AVDD = 3V)	-	1		mS

Chip Packaging



SYMBOL	MILLIRMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	---	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F Carrier Dimensions	150X150		

Figure 5. QFN32 Package Dimensions



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Figure 6. SOP16 Package Dimensions